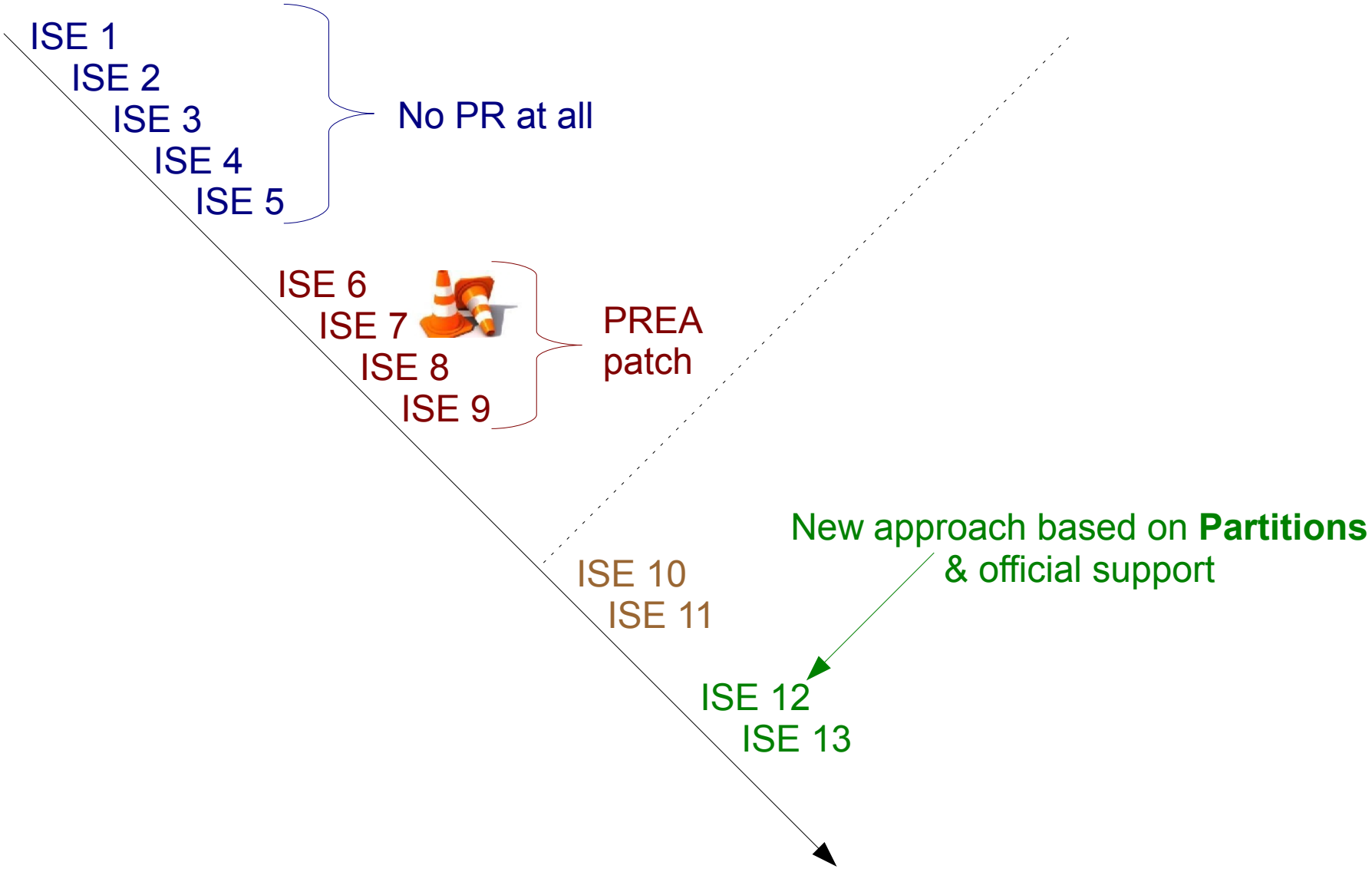
IRI Frankfurt

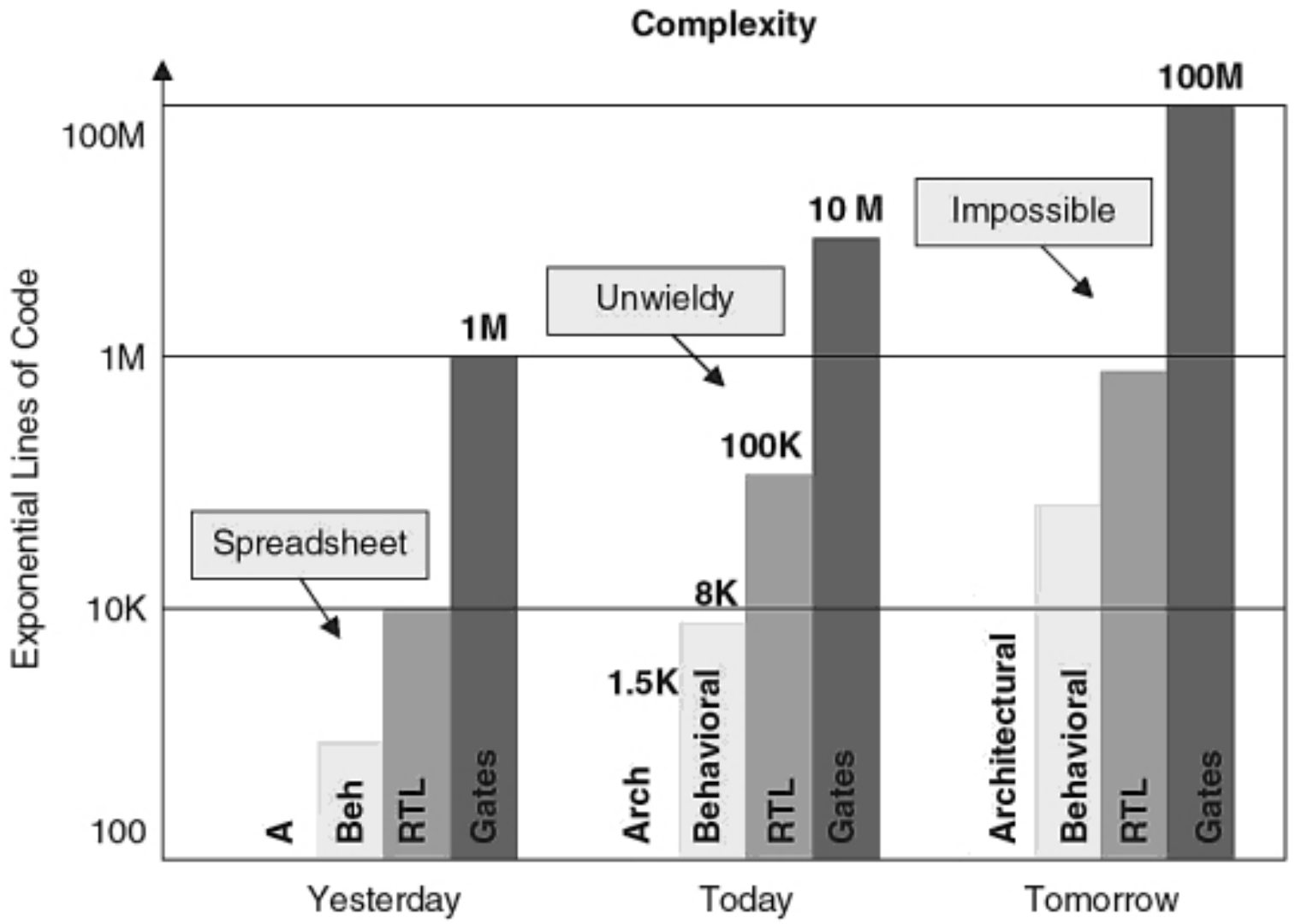
Norbert Abel, Christian Stüllein, Udo Kebschull

Partitions and Partial Reconfiguration

History


ISE 1
ISE 2
ISE 3
ISE 4
ISE 5
No PR at all
ISE 6
ISE 7
ISE 8
ISE 9
PREA
patch
New approach based on **Partitions**
& official support
ISE 10
ISE 11
ISE 12
ISE 13

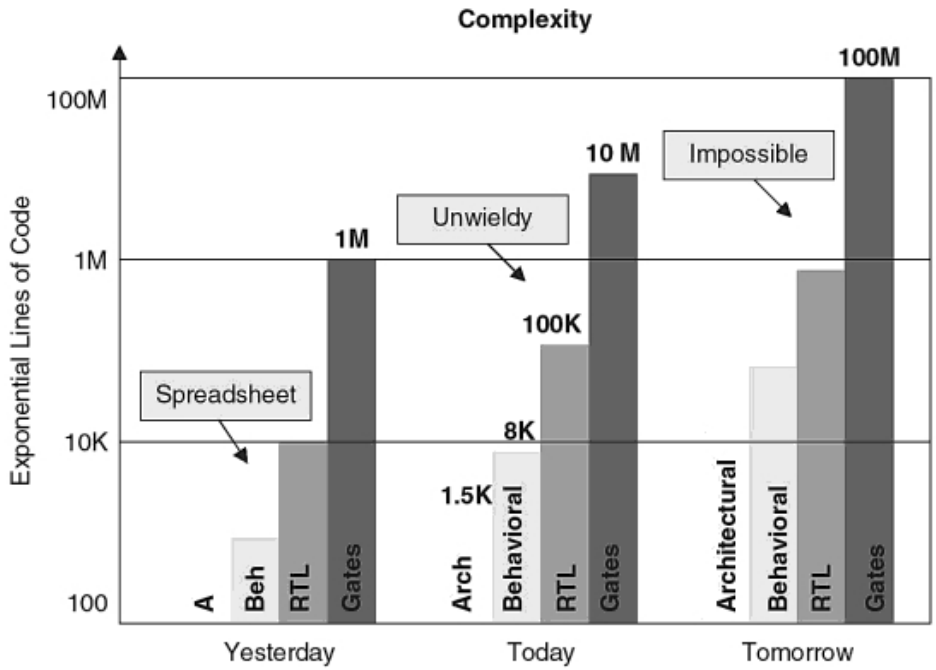
Motivation



Black, Donovan, Bunton, Keist
„SystemC: From the Ground Up“

Motivation

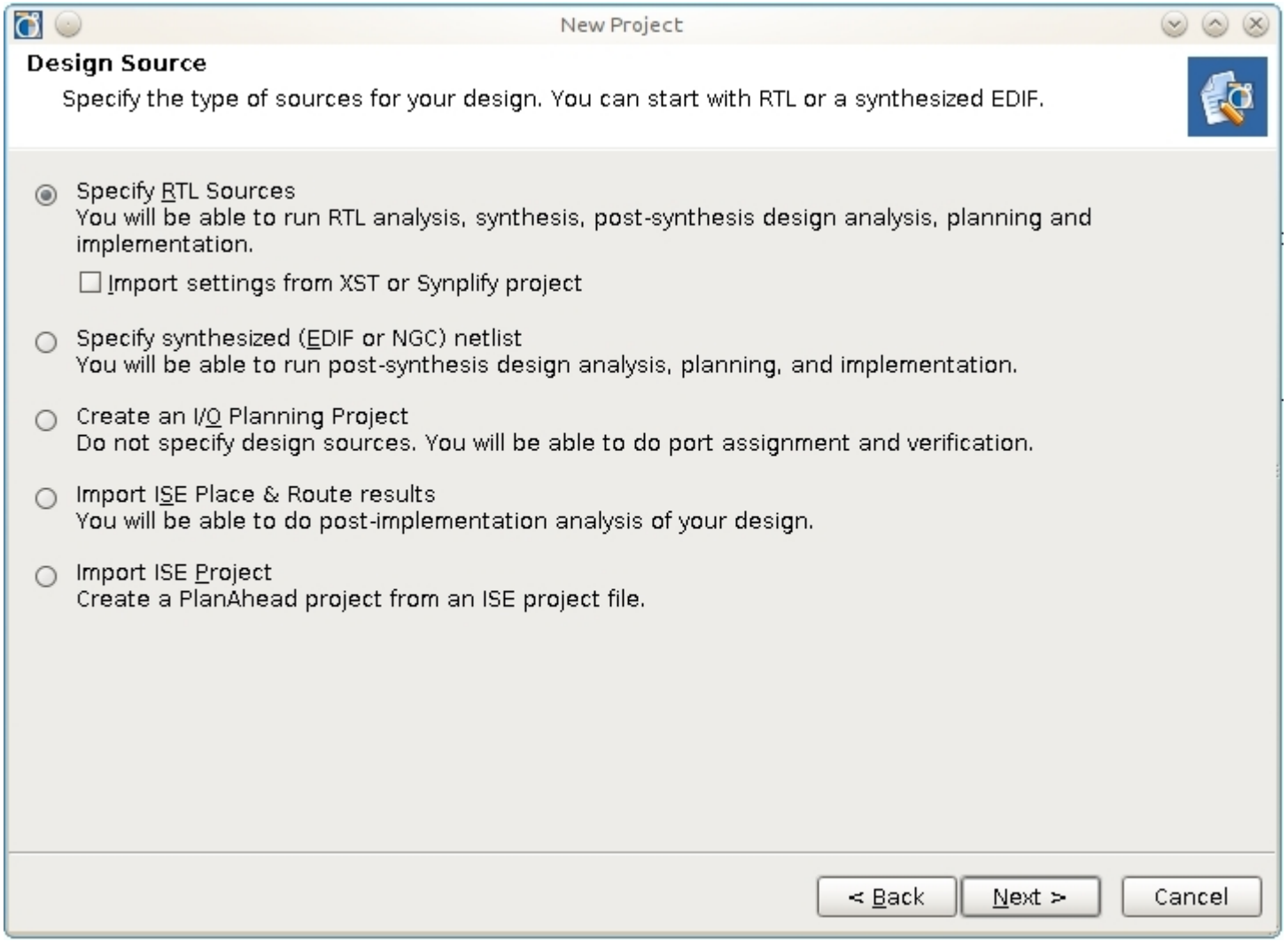
- High Level Synthesis
- Team Design
- Hierarchical Design & Re-Use



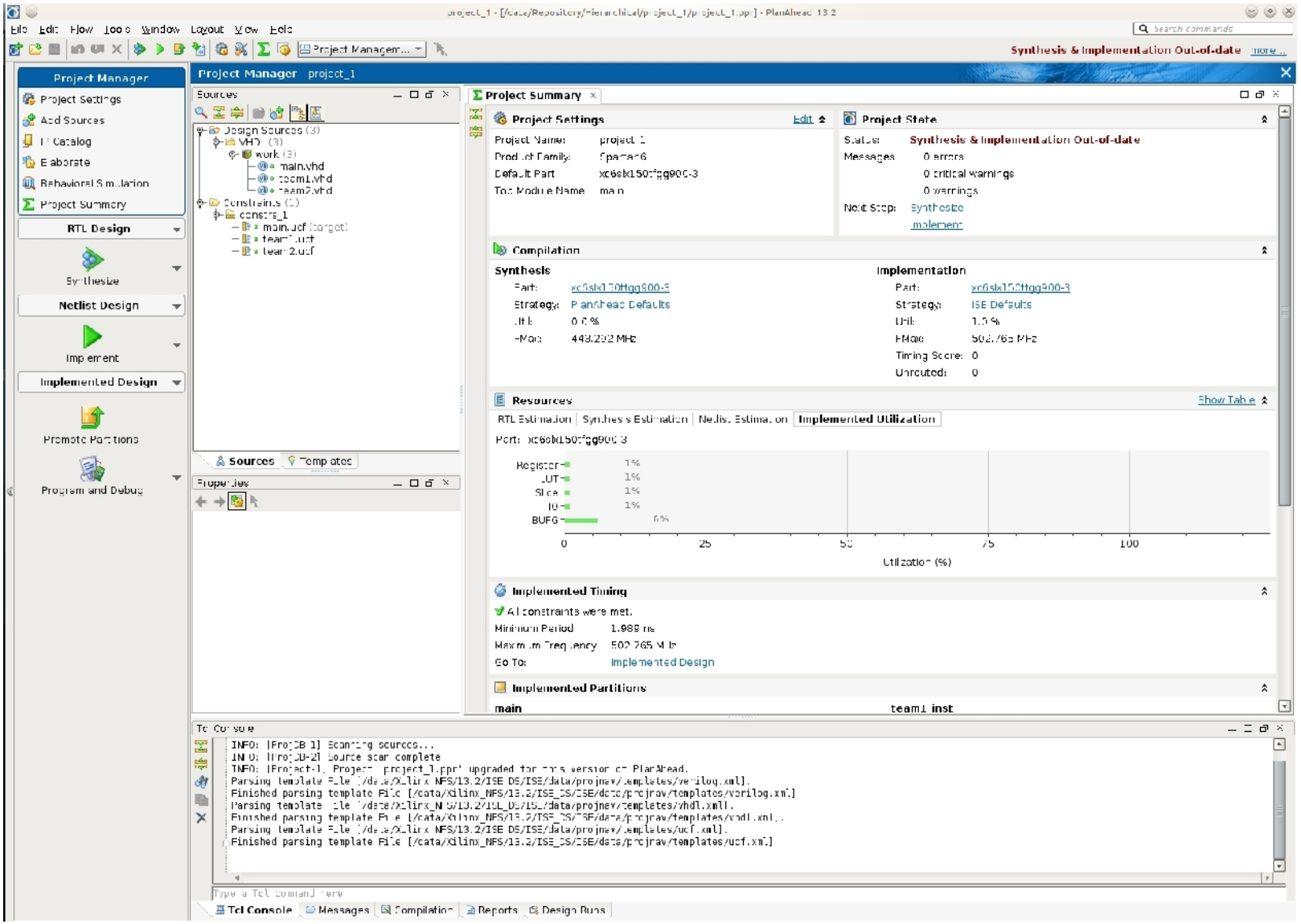
Partitions

Partitions are Xilinx's approach to Team Design and Hierarchical Design

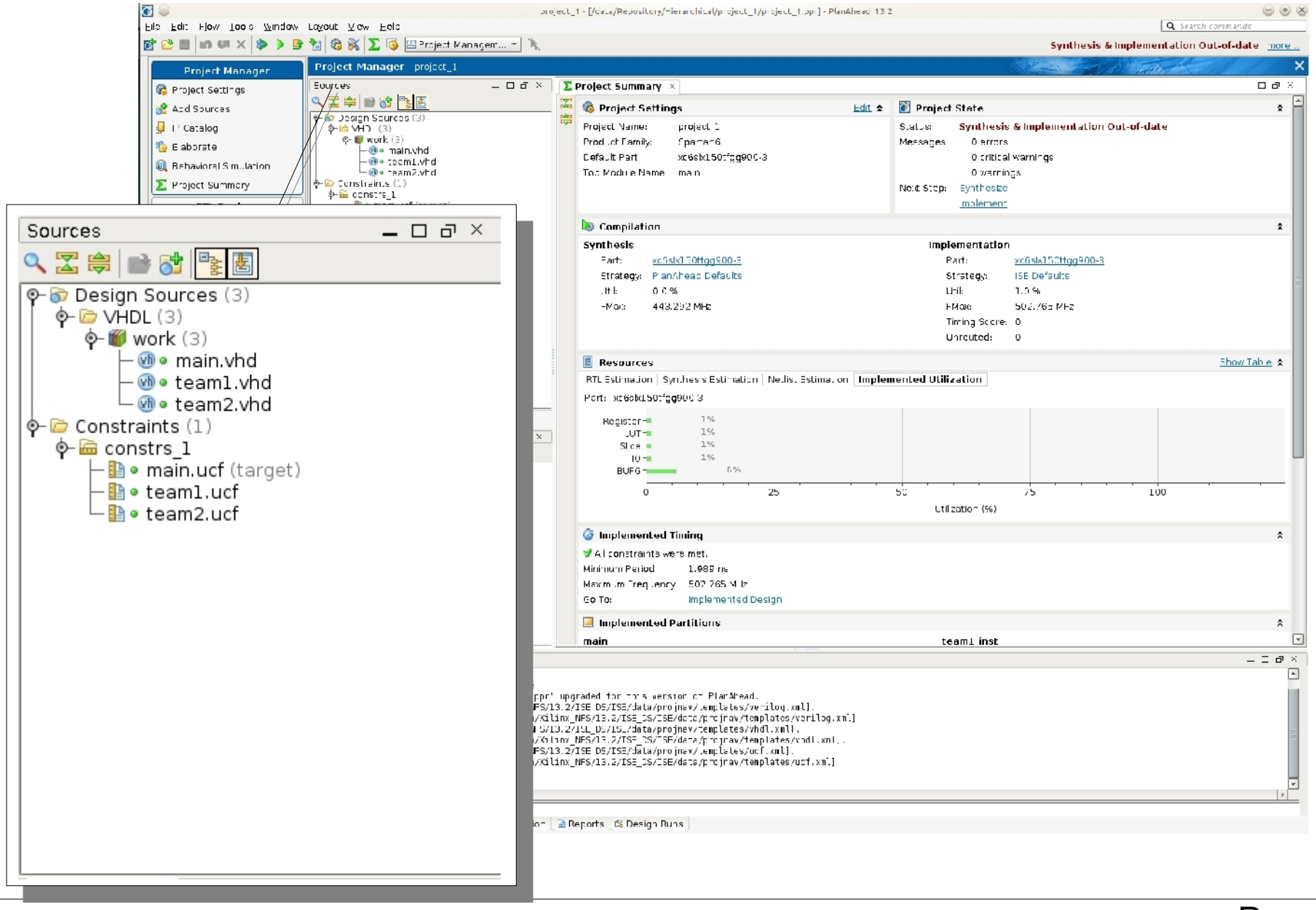
Tool: PlanAhead



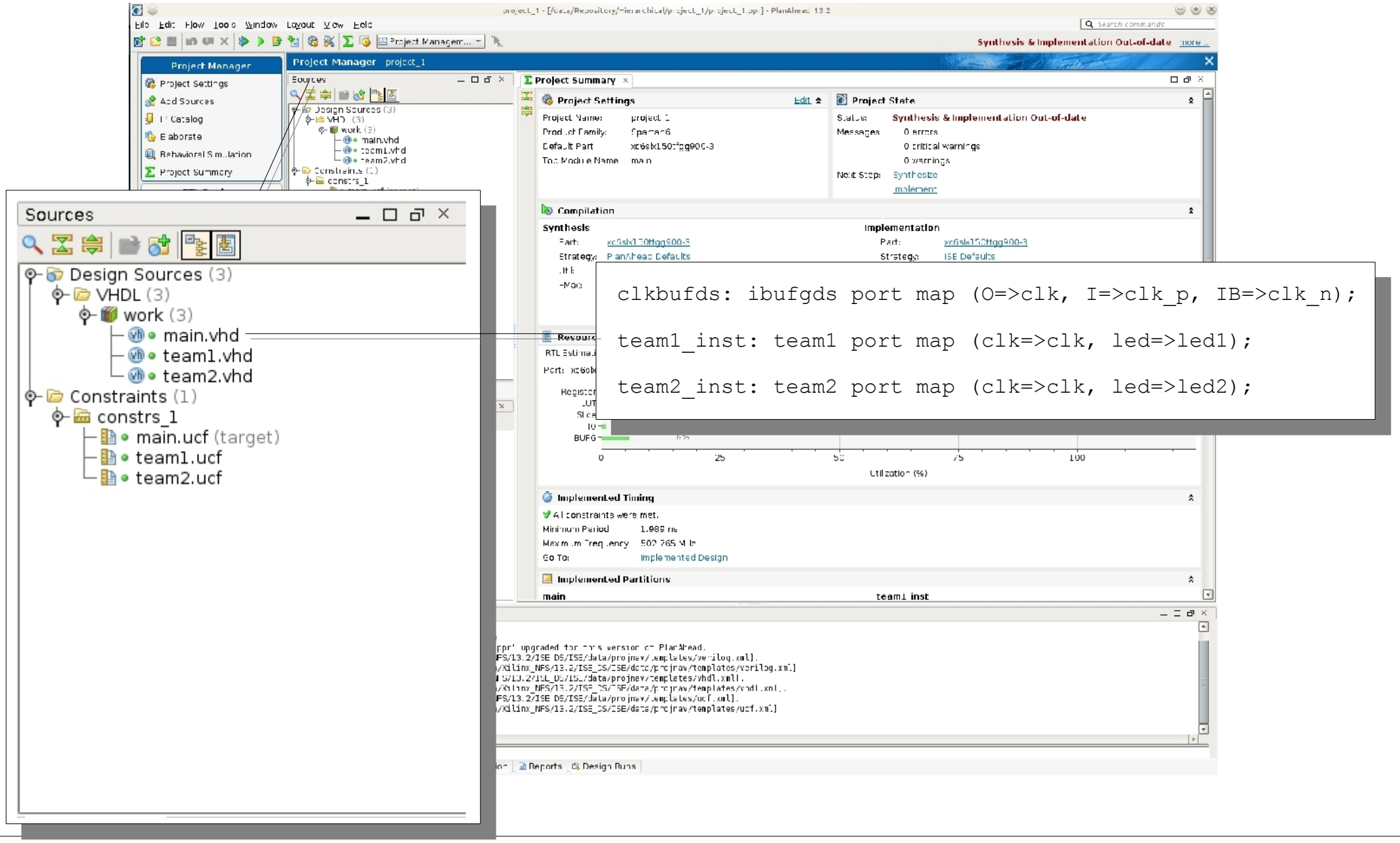
RTL Project


Project Manager
Project Settings
Add Sources
IP Catalog
Elaborate
Behavioral Simulation
Project Summary
RTL Design
Synthesize
Netlist Design
Implement
Implemented Design
Promote Partitions
Program and Debug
Project Manager project_1
Sources
Design Sources (3)
VHD (3)
work (3)
main.vhd
team1.vhd
team2.vhd
Constraints (1)
constrs_1
main.ucf (target)
team1.ucf
team2.ucf
Sources
Templates
Properties
Project Summary
Project Settings
Edit
Project Name: project_1
Product Family: Spartan6
Default Part: xc6slx150t-fgg900-3
Top Module Name: main
Project State
Status: Synthesis & Implementation Out-of-date
Messages: 0 errors
0 critical warnings
0 warnings
Next Step: Synthesize
Implement
Compilation
Synthesis
Part: xc6slx150tfgg900-3
Strategy: PlanAhead Defaults
Implementation
Part: xc6slx150tfgg900-3
Strategy: ISE Defaults
Resources
Show Table
RTL Estimation
Synthesis Estimation
Netlist Estimation
Implemented Utilization
Register
LUT
Slice
IO
BUFG
Utilization (%)
Implemented Timing
All constraints were met.
Minimum Period: 1.988 ns
Maximum Frequency: 502.765 MHz
Go To: Implemented Design
Implemented Partitions
main
team1 inst
Tcl Console
INFO: [Project 1] Scanning sources...
INFO: [Project 2] Source scan complete
INFO: [Project 1] Project 'project_1.ppr' upgraded for this version of PlanAhead.
Parsing template file '/data/Xilinx_NFS/13.2/ISE_DS/ISE/data/projnav/templates/verilog.xml'.
Finished parsing template file [/data/Xilinx_NFS/13.2/ISE_DS/ISE/data/projnav/templates/verilog.xml]
Parsing template file '/data/Xilinx_NFS/13.2/ISE_DS/ISE/data/projnav/templates/vhdl.xml'.
Finished parsing template file [/data/Xilinx_NFS/13.2/ISE_DS/ISE/data/projnav/templates/vhdl.xml]
Parsing template file '/data/Xilinx_NFS/13.2/ISE_DS/ISE/data/projnav/templates/ucf.xml'.
Finished parsing template file [/data/Xilinx_NFS/13.2/ISE_DS/ISE/data/projnav/templates/ucf.xml]
Type a Tcl command here
Tcl Console
Messages
Compilation
Reports
Design Runs

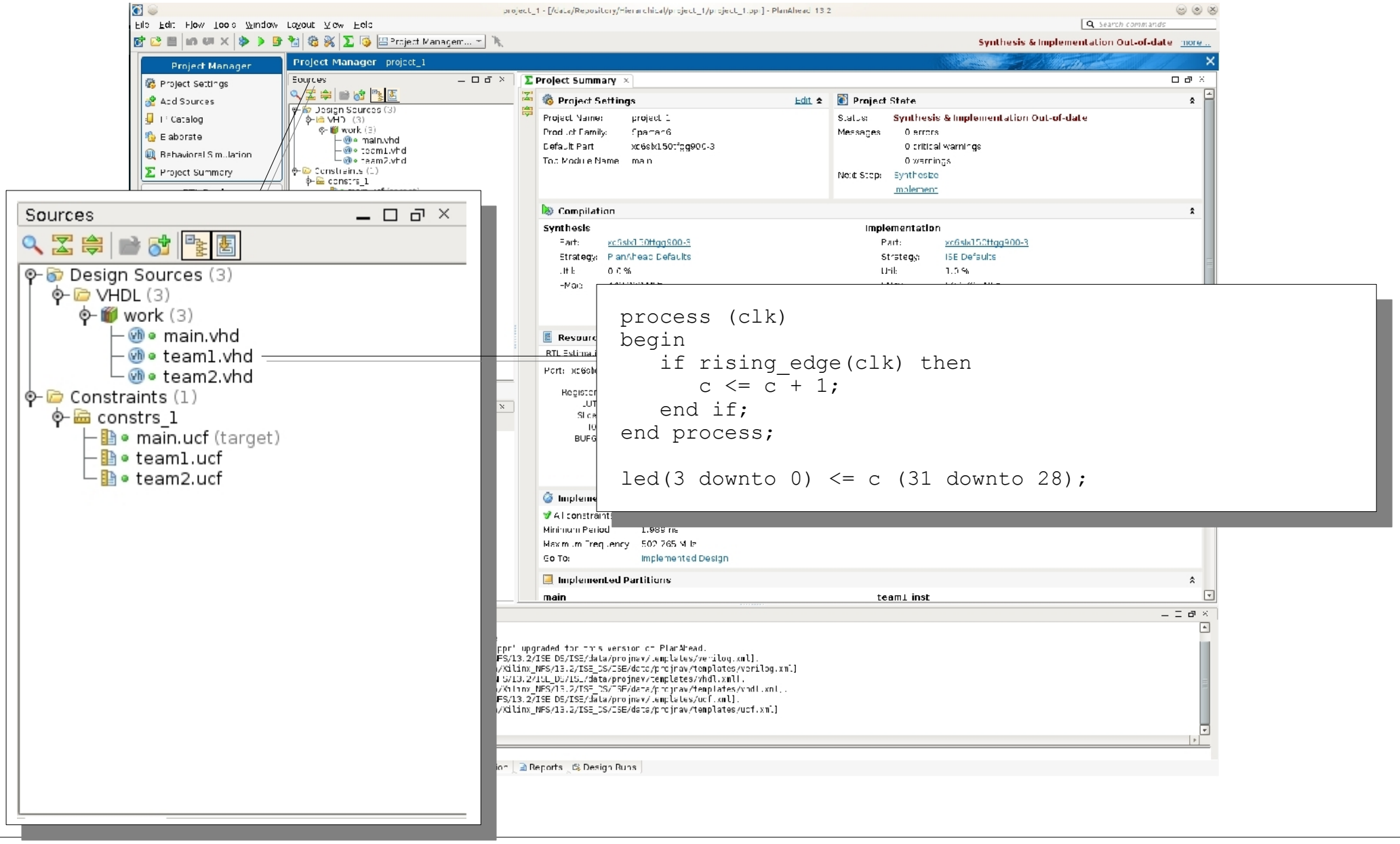
RTL Project


Project Manager
Project Settings
Add Sources
Elaborate
Project Summary
Sources
Design Sources (3)
VHDL (3)
work (3)
main.vhd
team1.vhd
team2.vhd
Constraints (1)
constrs_1
main.ucf (target)
team1.ucf
team2.ucf
Project Summary
Project Settings
Project State
Synthesis & Implementation Out-of-date
Compilation
Synthesis
Implementation
Resources
Implemented Timing
All constraints were met.
Implemented Partitions
Reports
Design Runs

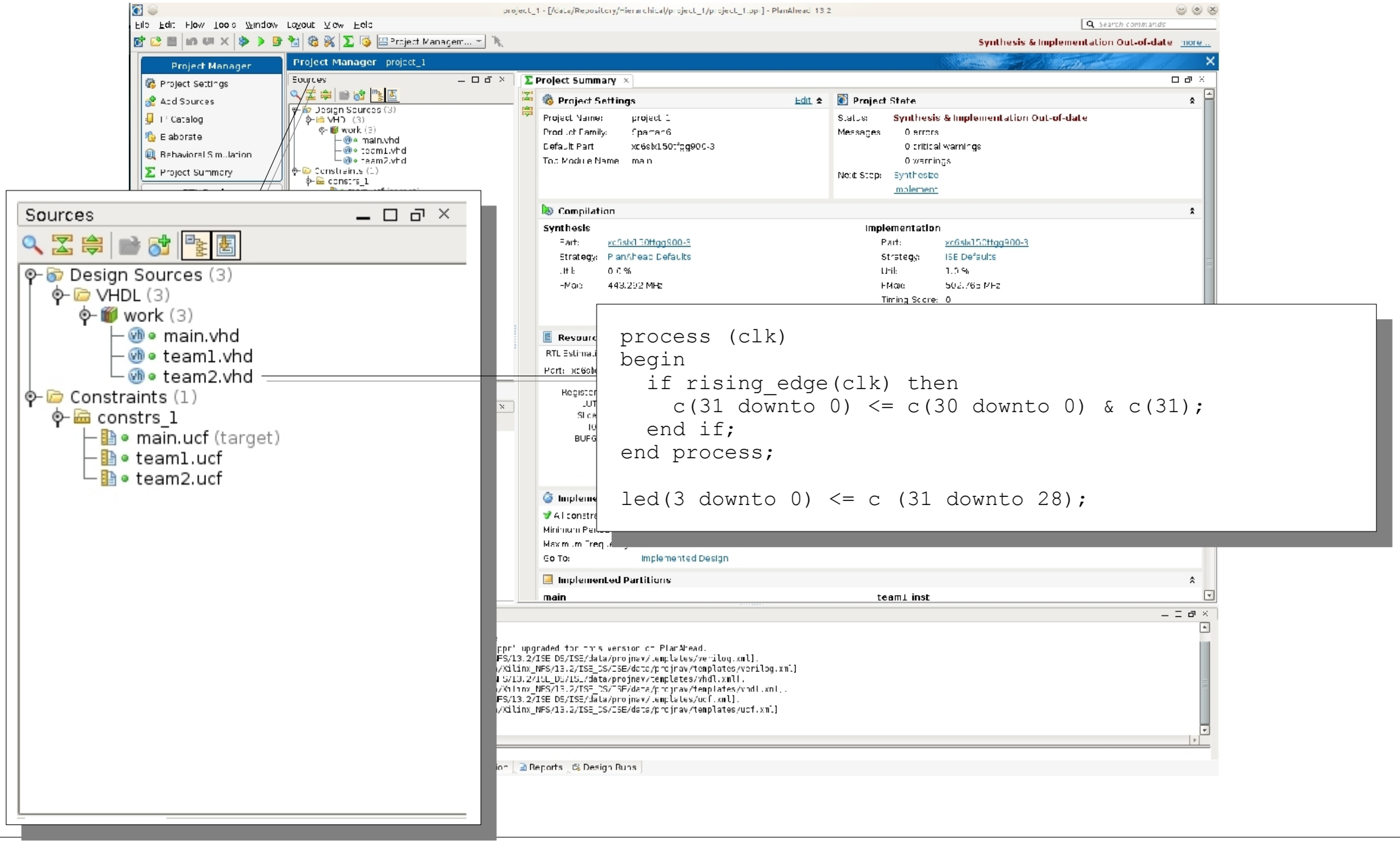
RTL Project


Sources
Design Sources (3)
VHDL (3)
work (3)
main.vhd
team1.vhd
team2.vhd
Constraints (1)
constrs_1
main.ucf (target)
team1.ucf
team2.ucf
clkbufds: ibufgds port map (O=>clk, I=>clk_p, IB=>clk_n);
team1_inst: team1 port map (clk=>clk, led=>led1);
team2_inst: team2 port map (clk=>clk, led=>led2);

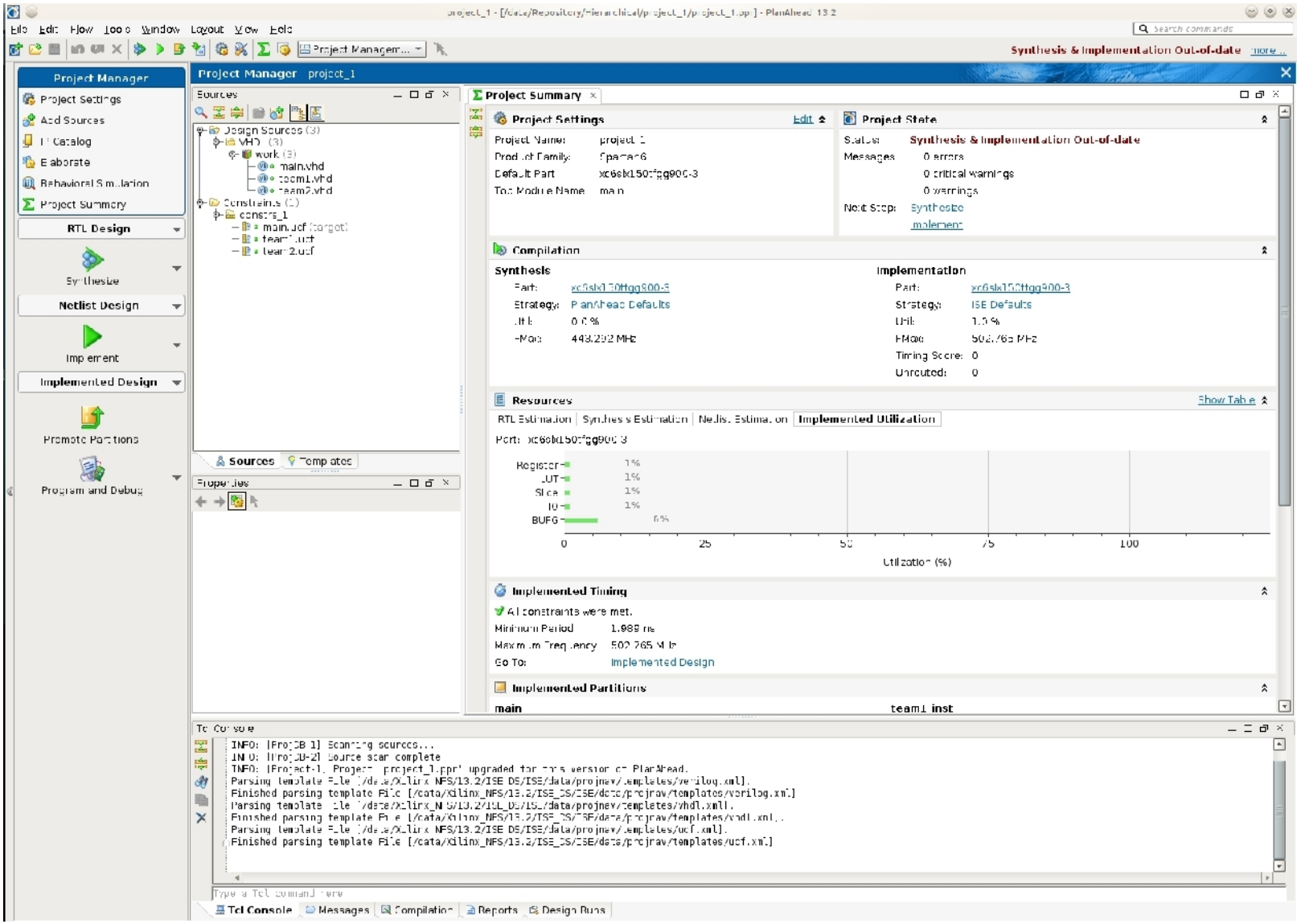
RTL Project


Sources
Design Sources (3)
VHDL (3)
work (3)
main.vhd
team1.vhd
team2.vhd
Constraints (1)
constrs_1
main.ucf (target)
team1.ucf
team2.ucf
process (clk)
begin
if rising_edge(clk) then
c <= c + 1;
end if;
end process;
led(3 downto 0) <= c (31 downto 28);

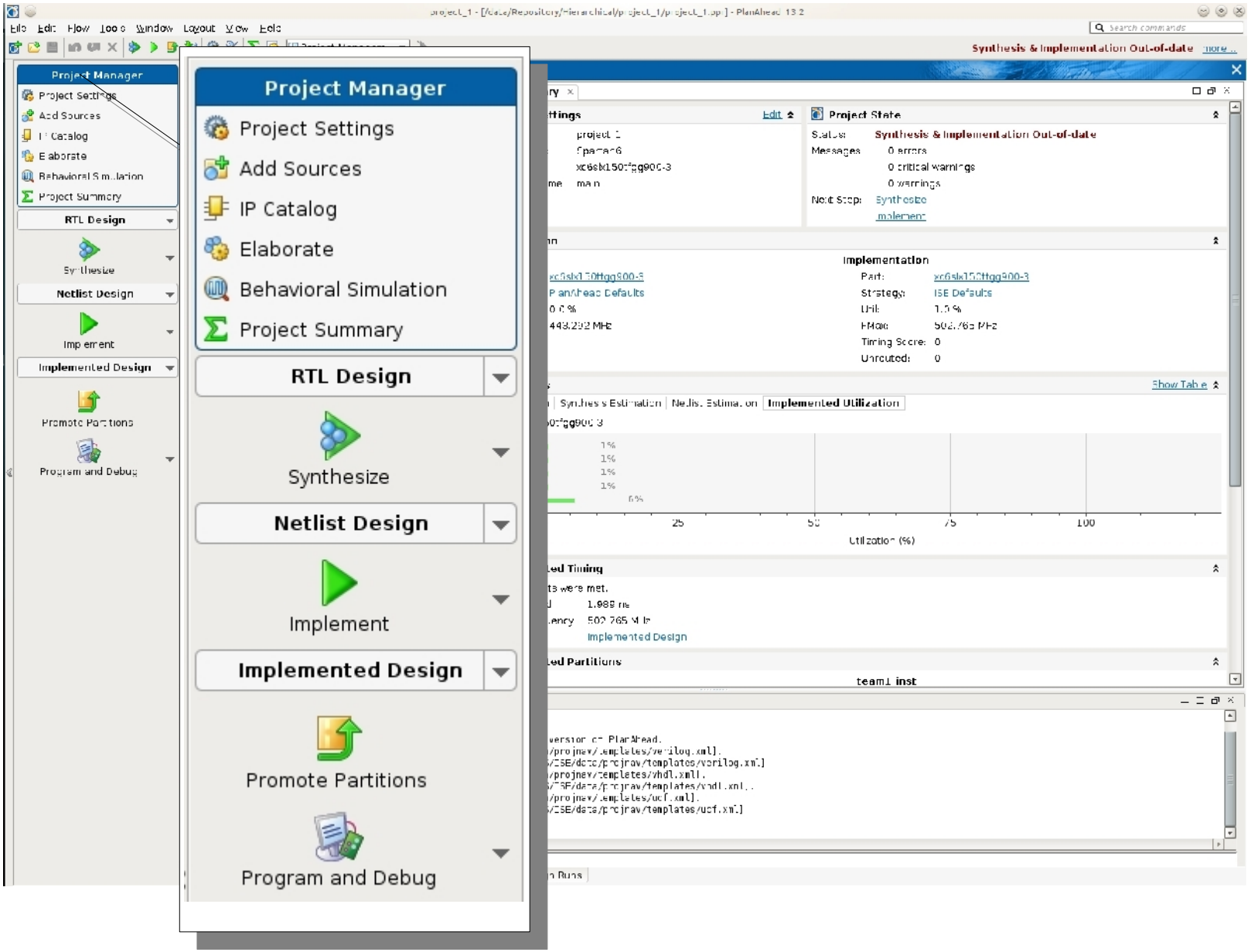
RTL Project


Sources
Design Sources (3)
VHDL (3)
work (3)
main.vhd
team1.vhd
team2.vhd
Constraints (1)
constrs_1
main.ucf (target)
team1.ucf
team2.ucf
process (clk)
begin
if rising_edge(clk) then
c(31 downto 0) <= c(30 downto 0) & c(31);
end if;
end process;
led(3 downto 0) <= c (31 downto 28);

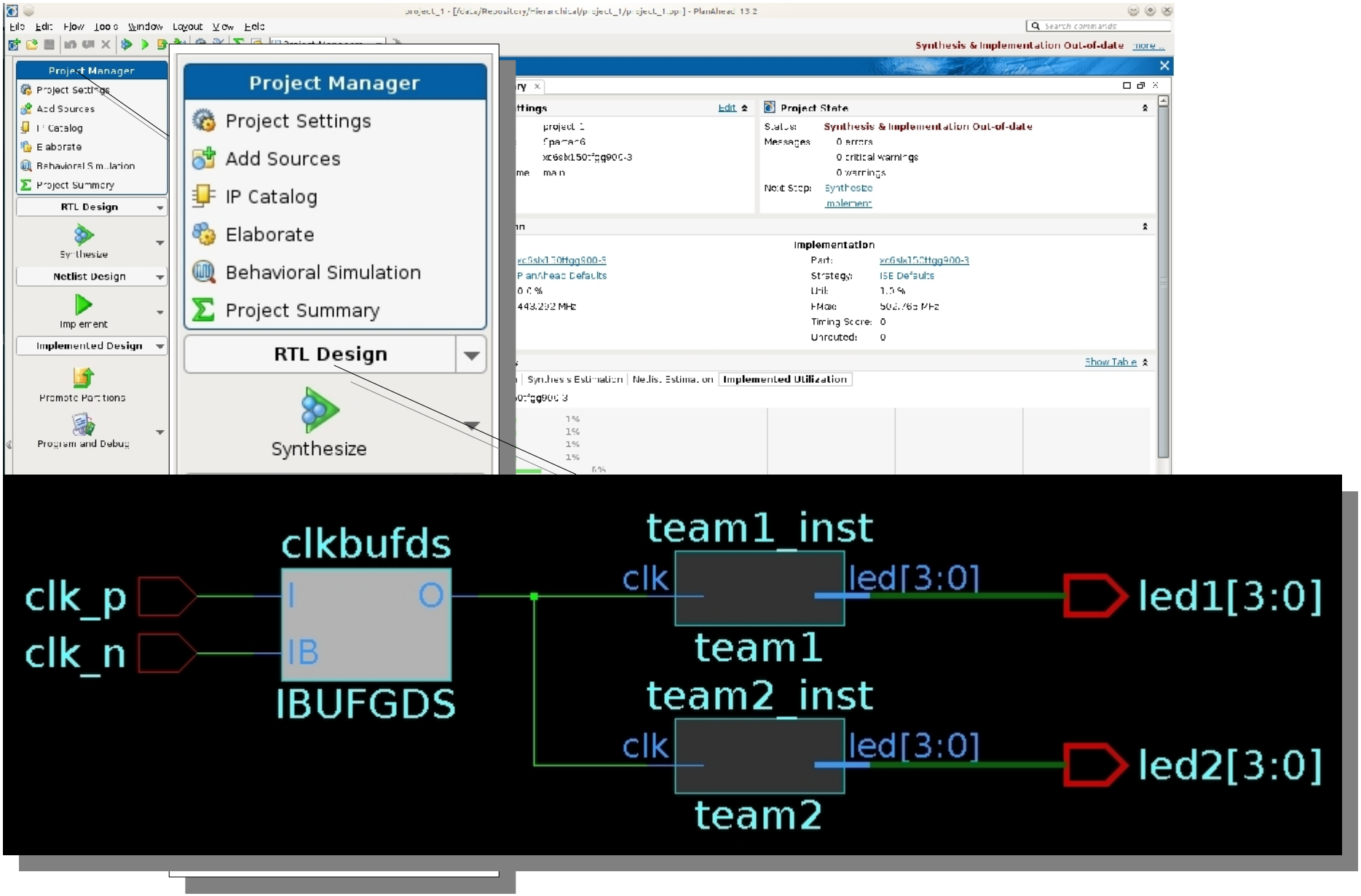
RTL Project


Project Manager
Project Settings
Add Sources
IP Catalog
Elaborate
Behavioral Simulation
Project Summary
RTL Design
Synthesize
Netlist Design
Implement
Implemented Design
Promote Partitions
Program and Debug
Project Manager project_1
Sources
Design Sources (3)
VHD (3)
work (3)
main.vhd
team1.vhd
team2.vhd
Constraints (1)
constrs_1
main.ucf (target)
team1.ucf
team2.ucf
Sources
Templates
Properties
Project Summary
Project Settings
Edit
Project Name: project_1
Product Family: Spartan6
Default Part: xc6slx150t-fgg900-3
Top Module Name: main
Project State
Status: Synthesis & Implementation Out-of-date
Messages: 0 errors
0 critical warnings
0 warnings
Next Step: Synthesize
Implement
Compilation
Synthesis
Part: xc6slx150tfgg900-3
Strategy: PlanAhead Defaults
LUT: 0.0 %
FMax: 448.292 MHz
Implementation
Part: xc6slx150tfgg900-3
Strategy: ISE Defaults
LUT: 1.0 %
FMax: 502.765 MHz
Timing Score: 0
Unrouted: 0
Resources
Show Table
RTL Estimation
Synthesis Estimation
Netlist Estimation
Implemented Utilization
Part: xc6slx150tfgg900-3
Register 1%
LUT 1%
Slice 1%
IO 1%
BUFG 6%
0
25
50
75
100
Utilization (%)
Implemented Timing
All constraints were met.
Minimum Period 1.988 ns
Maximum Frequency 502.765 MHz
Go To: Implemented Design
Implemented Partitions
main
team1_inst
Tcl Console
INFO: [Project 1-1] Project project_1.ppr upgraded from an older version of PlanAhead.
Finished parsing template file [/data/Xilinx_NFS/13.2/ISE_DS/ISE/data/projnav/templates/verilog.xml]
Finished parsing template file [/data/Xilinx_NFS/13.2/ISE_DS/ISE/data/projnav/templates/vhdl.xml]
Finished parsing template file [/data/Xilinx_NFS/13.2/ISE_DS/ISE/data/projnav/templates/ucf.xml]
Type a Tcl command here
Tcl Console
Messages
Compilation
Reports
Design Runs

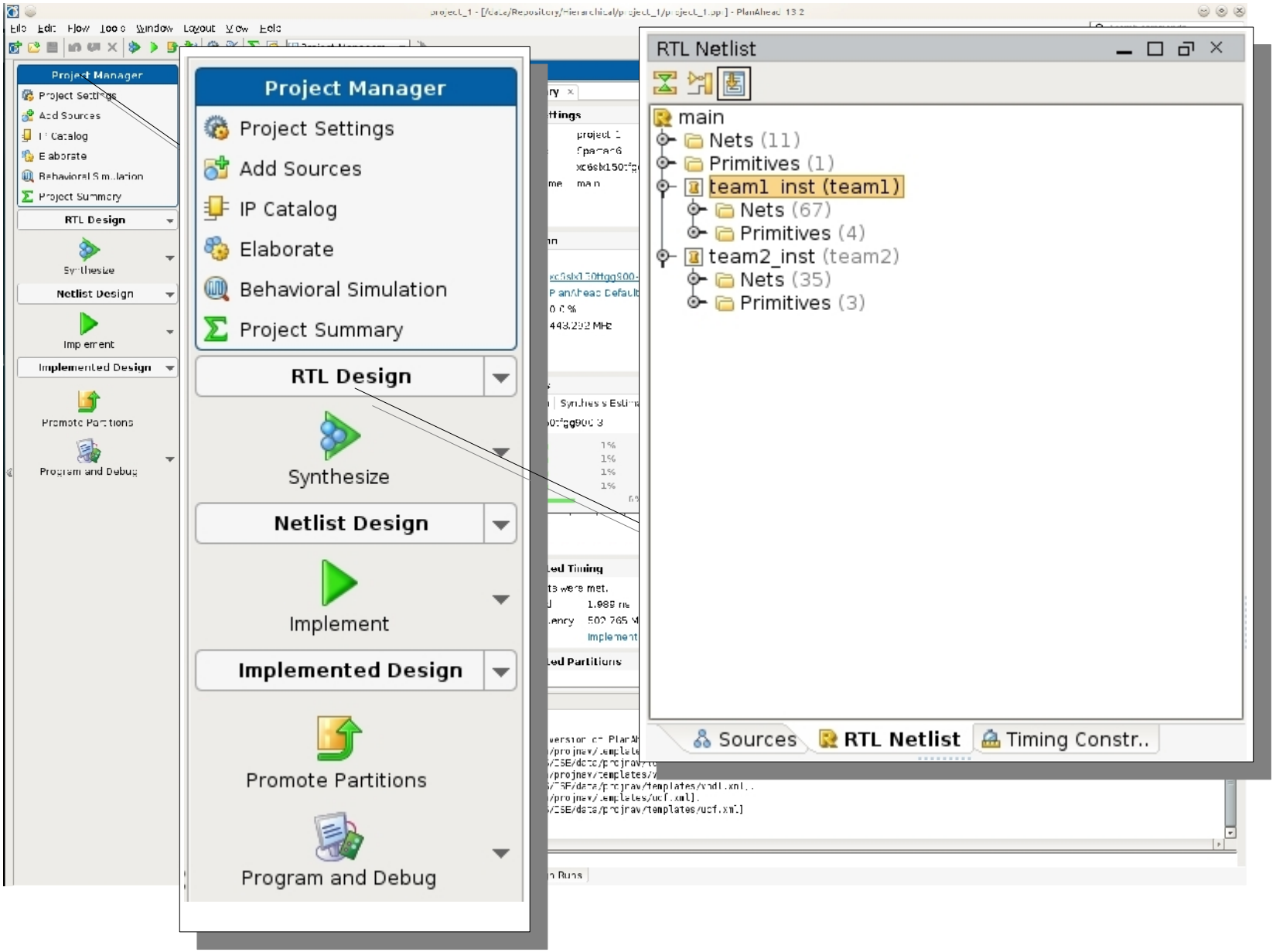
RTL Project


Project Manager
Project Settings
Add Sources
IP Catalog
Elaborate
Behavioral Simulation
Project Summary
RTL Design
Synthesize
Netlist Design
Implement
Implemented Design
Promote Partitions
Program and Debug

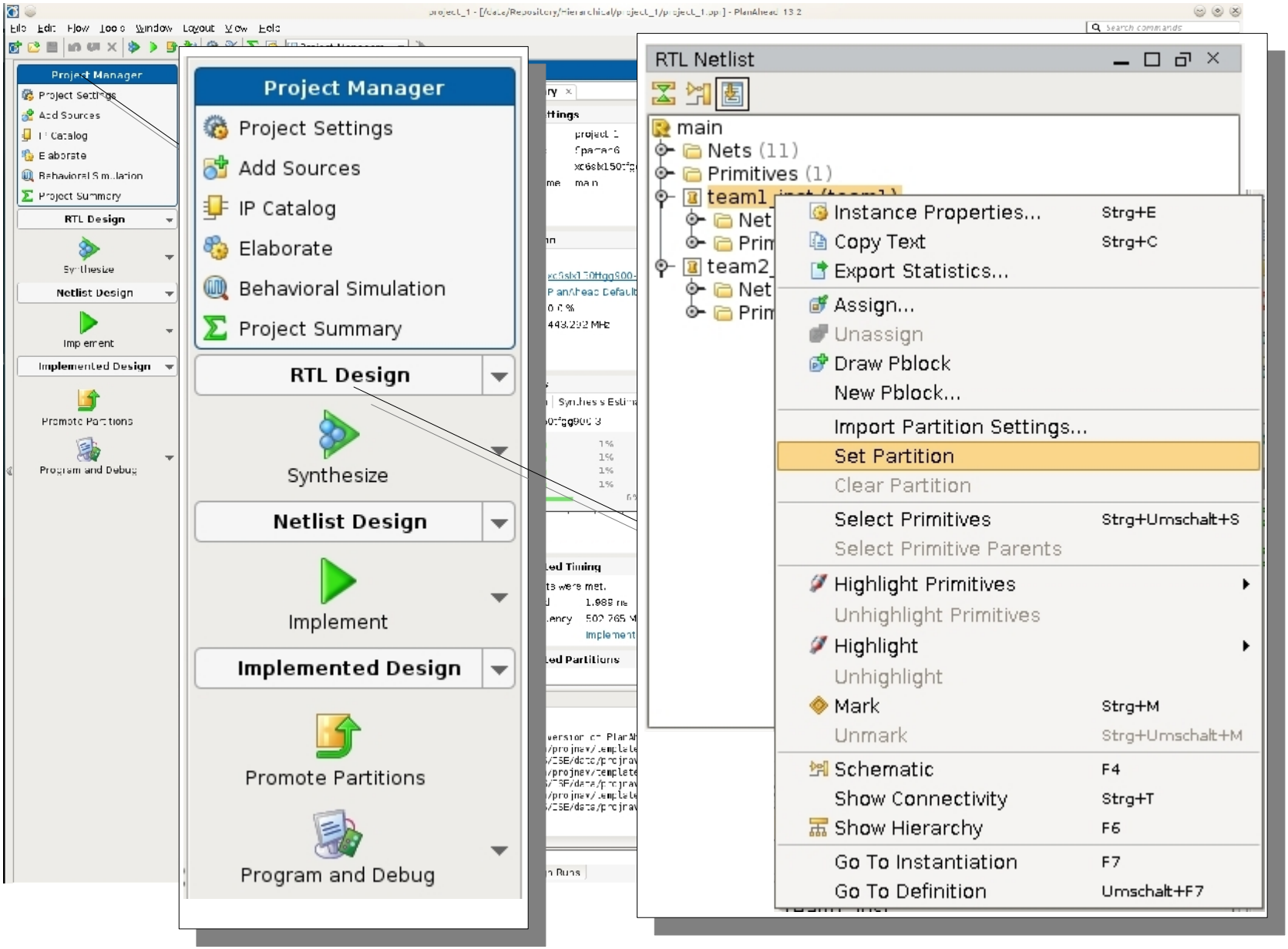
RTL Project


Project Manager
Project Settings
Add Sources
IP Catalog
Elaborate
Behavioral Simulation
Project Summary
RTL Design
Synthesize
clkbufds
clk_p
clk_n
I
IB
O
IBUFGDS
team1_inst
clk
led[3:0]
team1
led1[3:0]
team2_inst
clk
led[3:0]
team2
led2[3:0]

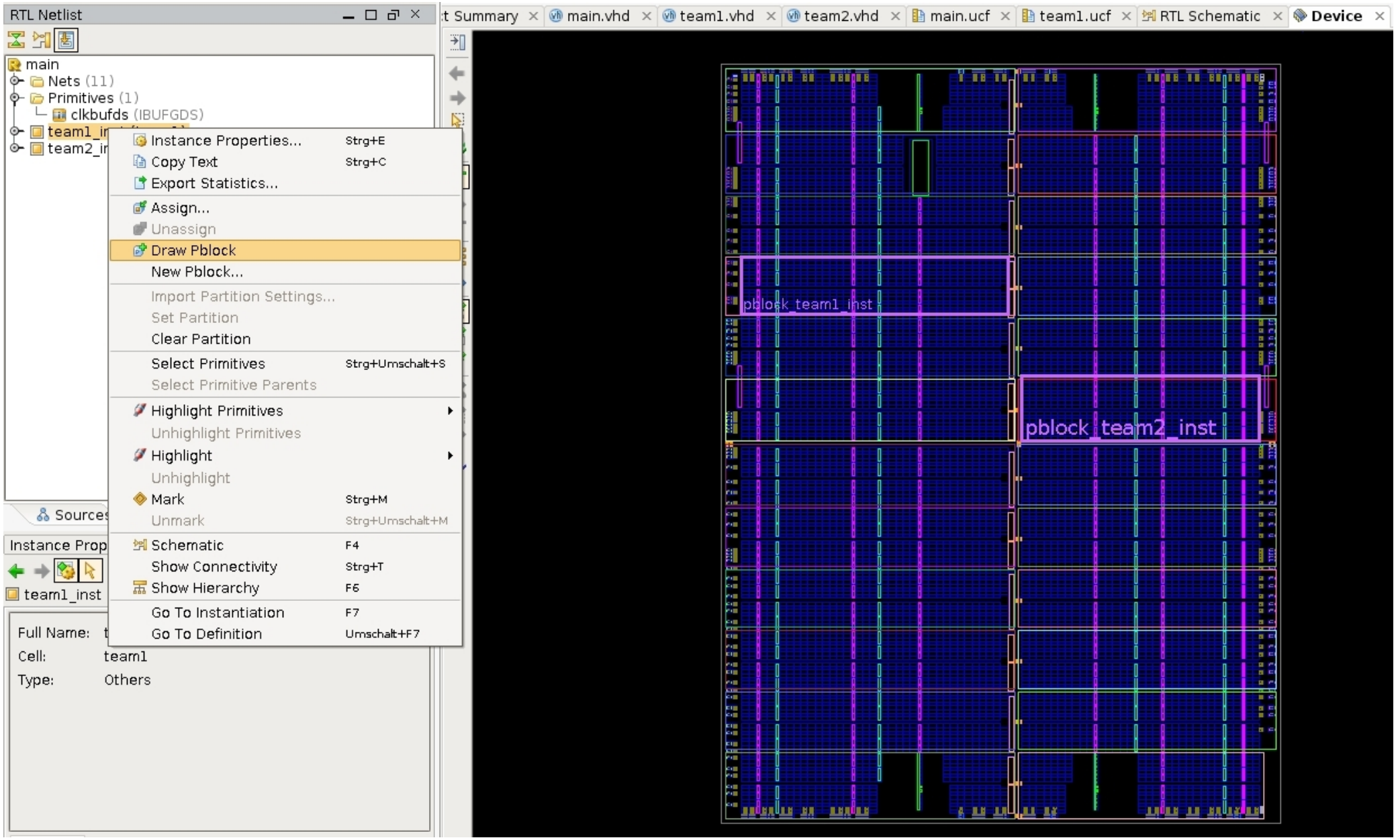
RTL Project


Project Manager
Project Settings
Add Sources
IP Catalog
Elaborate
Behavioral Simulation
Project Summary
RTL Design
Synthesize
Netlist Design
Implement
Implemented Design
Promote Partitions
Program and Debug
RTL Netlist
main
Nets (11)
Primitives (1)
team1_inst (team1)
Nets (67)
Primitives (4)
team2_inst (team2)
Nets (35)
Primitives (3)
Sources
RTL Netlist
Timing Constr..

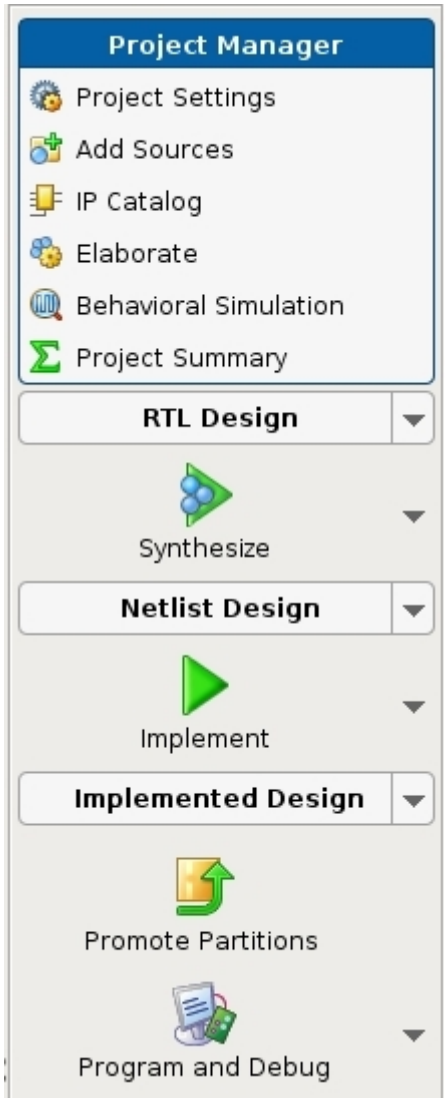
RTL Project


Project Manager
Project Settings
Add Sources
IP Catalog
Elaborate
Behavioral Simulation
Project Summary
RTL Design
Synthesize
Netlist Design
Implement
Implemented Design
Promote Partitions
Program and Debug
RTL Netlist
main
Nets (11)
Primitives (1)
team1
team2
Instance Properties... Strg+E
Copy Text Strg+C
Export Statistics...
Assign...
Unassign
Draw Pblock
New Pblock...
Import Partition Settings...
Set Partition
Clear Partition
Select Primitives Strg+Umschalt+S
Select Primitive Parents
Highlight Primitives
Unhighlight Primitives
Highlight
Unhighlight
Mark Strg+M
Unmark Strg+Umschalt+M
Schematic F4
Show Connectivity Strg+T
Show Hierarchy F6
Go To Instantiation F7
Go To Definition Umschalt+F7

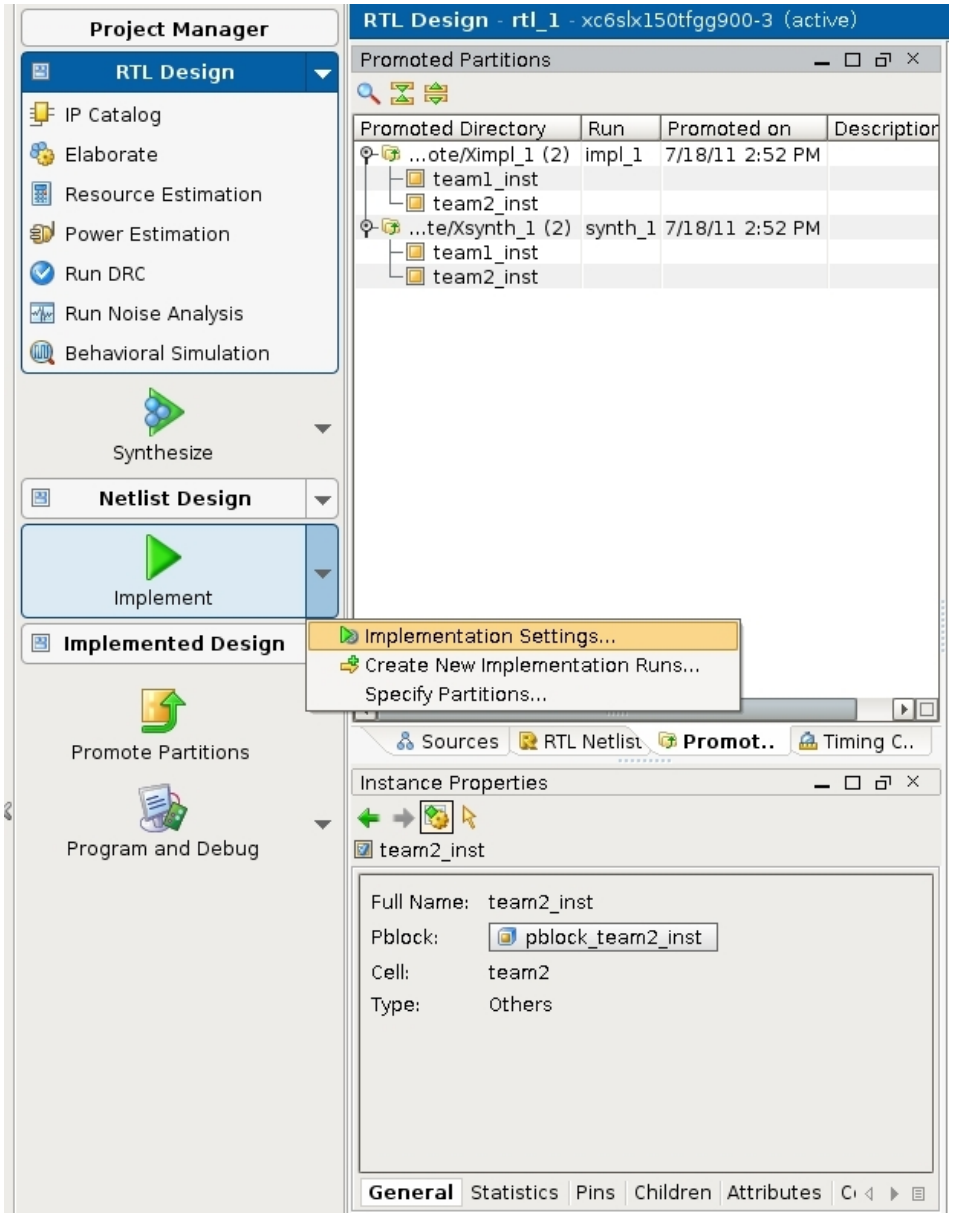
RTL Project


RTL Netlist
main
Nets (11)
Primitives (1)
clkbufds (IBUFGDS)
team1_inst
team2_inst
Instance Properties... Strg+E
Copy Text Strg+C
Export Statistics...
Assign...
Unassign
Draw Pblock
New Pblock...
Import Partition Settings...
Set Partition
Clear Partition
Select Primitives Strg+Umschalt+S
Select Primitive Parents
Highlight Primitives
Unhighlight Primitives
Highlight
Unhighlight
Mark Strg+M
Unmark Strg+Umschalt+M
Schematic F4
Show Connectivity Strg+T
Show Hierarchy F6
Go To Instantiation F7
Go To Definition Umschalt+F7
Sources
Instance Prop
team1_inst
Full Name:
Cell: team1
Type: Others
t Summary
main.vhd
team1.vhd
team2.vhd
main.ucf
team1.ucf
RTL Schematic
Device
pblock_team1_inst
pblock_team2_inst

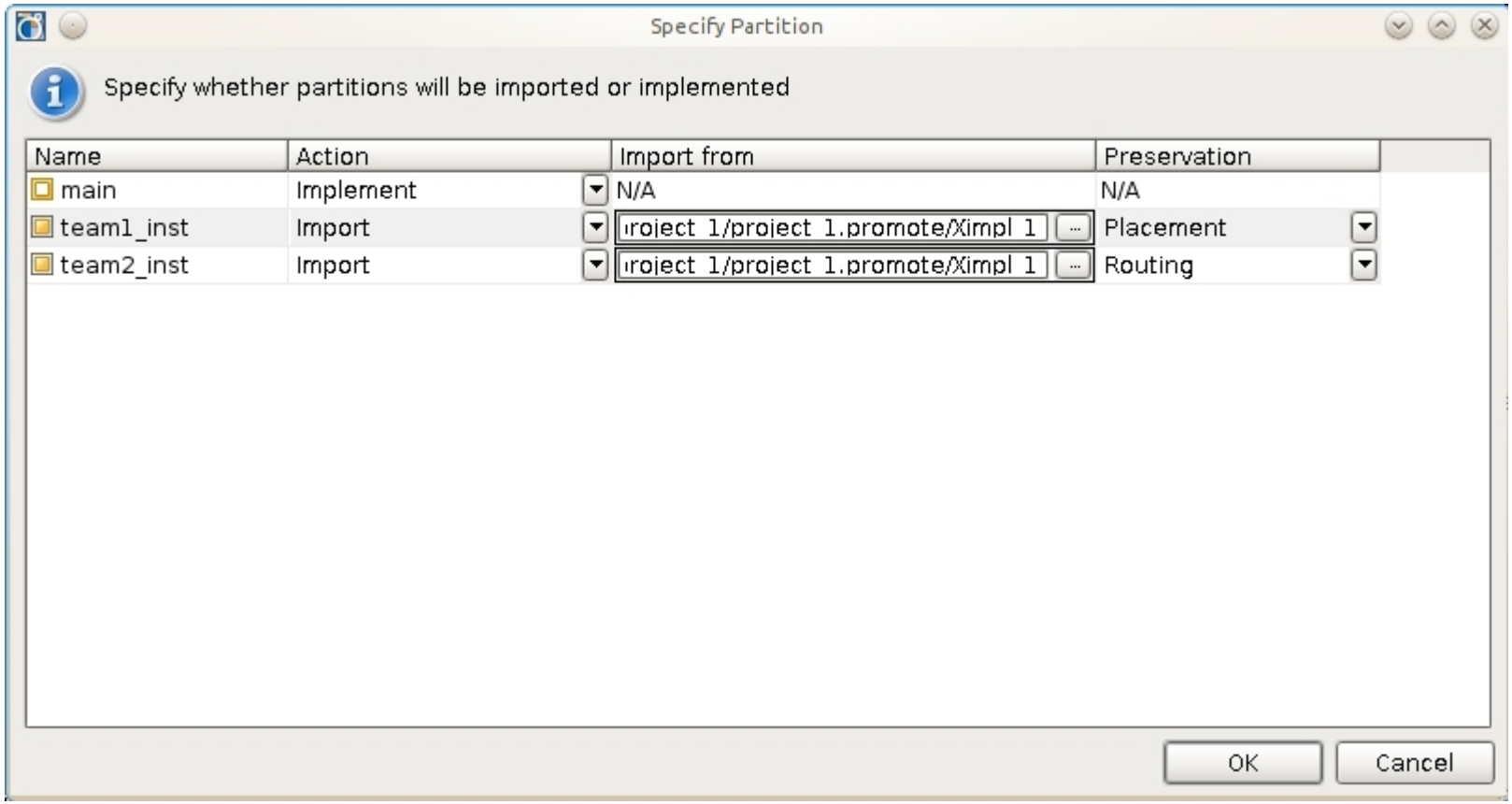
RTL Project


Project Manager
Project Settings
Add Sources
IP Catalog
Elaborate
Behavioral Simulation
Project Summary
RTL Design
Synthesize
Netlist Design
Implement
Implemented Design
Promote Partitions
Program and Debug

RTL Project


Project Manager
RTL Design
IP Catalog
Elaborate
Resource Estimation
Power Estimation
Run DRC
Run Noise Analysis
Behavioral Simulation
Synthesize
Netlist Design
Implement
Implemented Design
Promote Partitions
Program and Debug
RTL Design - rtl_1 - xc6slx150tfgg900-3 (active)
Promoted Partitions
Promoted Directory
Run
Promoted on
Description
...ote/Ximpl_1 (2)
impl_1
7/18/11 2:52 PM
team1_inst
team2_inst
...te/Xsynth_1 (2)
synth_1
7/18/11 2:52 PM
team1_inst
team2_inst
Implementation Settings...
Create New Implementation Runs...
Specify Partitions...
Sources
RTL Netlist
Promot..
Timing C..
Instance Properties
team2_inst
Full Name: team2_inst
Pblock: pblock_team2_inst
Cell: team2
Type: Others
General
Statistics
Pins
Children
Attributes

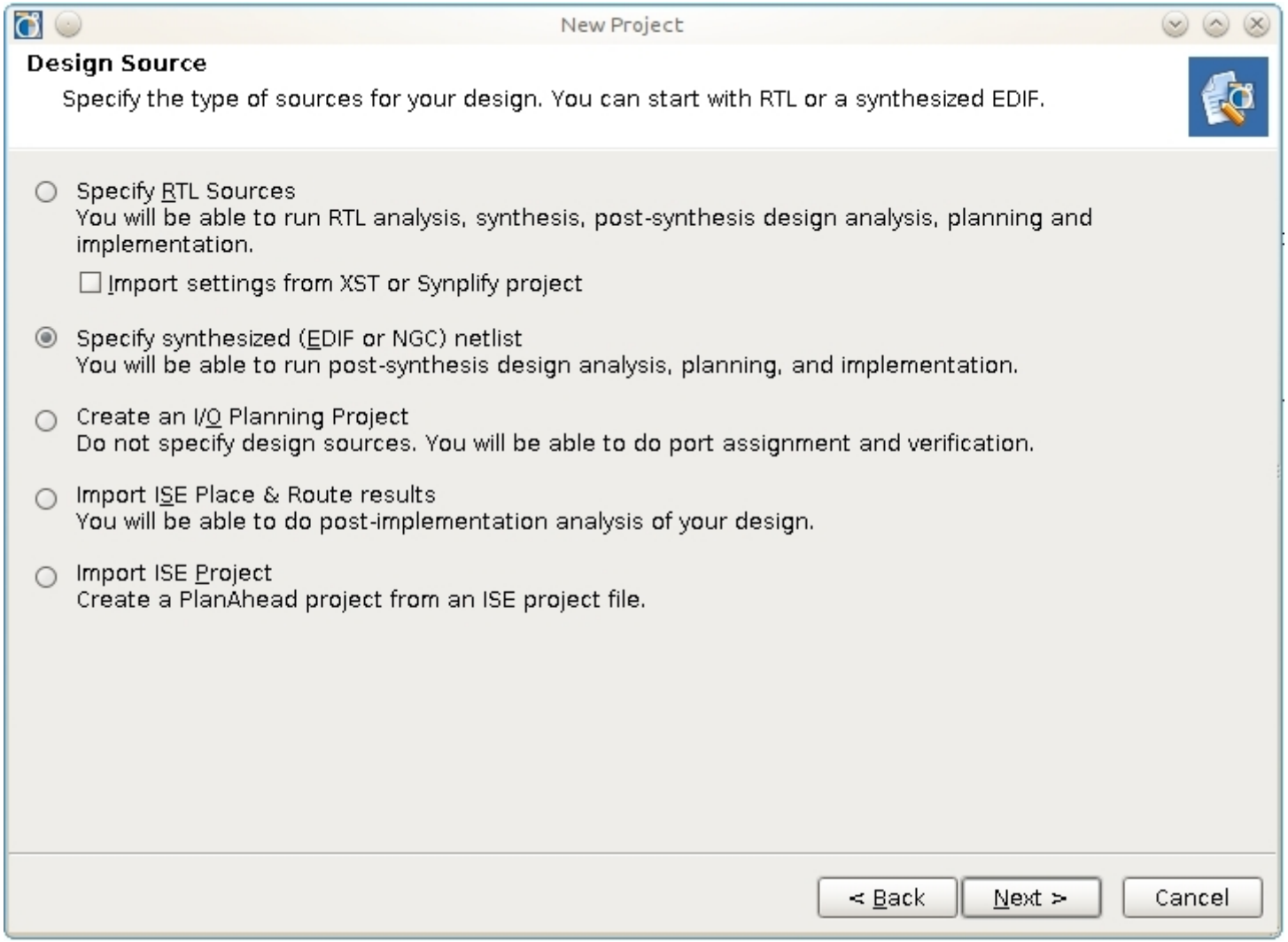
RTL Project



3 Levels of Design Preservation:

- Synthesis
- Placement
- Routing

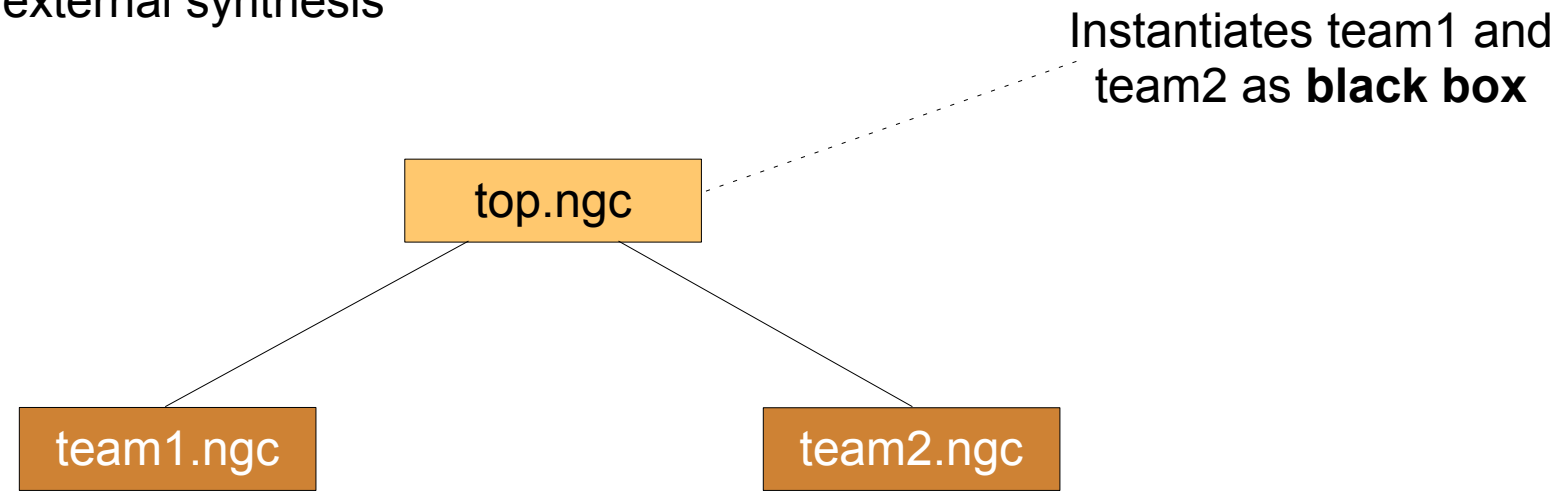
NGC Project


New Project
Design Source
Specify the type of sources for your design. You can start with RTL or a synthesized EDIF.
Specify RTL Sources
You will be able to run RTL analysis, synthesis, post-synthesis design analysis, planning and implementation.
Import settings from XST or Synplify project
Specify synthesized (EDIF or NGC) netlist
You will be able to run post-synthesis design analysis, planning, and implementation.
Create an I/O Planning Project
Do not specify design sources. You will be able to do port assignment and verification.
Import ISE Place & Route results
You will be able to do post-implementation analysis of your design.
Import ISE Project
Create a PlanAhead project from an ISE project file.
< Back
Next >
Cancel

NGC Project

Differences to the RTL Project:

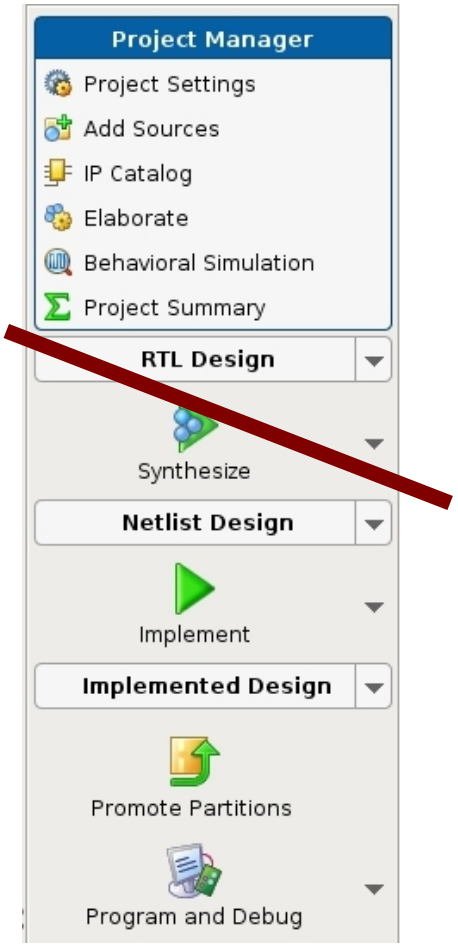
Sources: NGC files (netlists)
==> Requires external synthesis

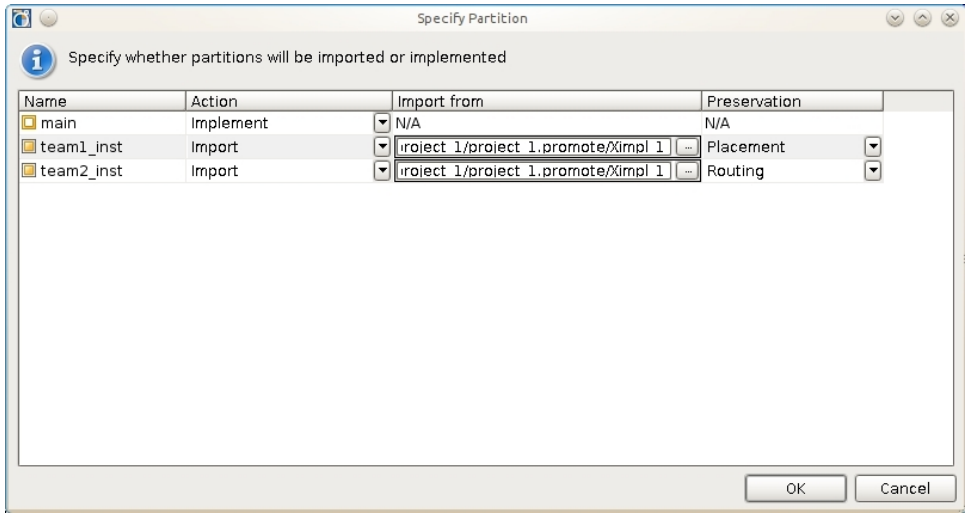


general Synthesis hints:
- deactivate automatically generated I/O buffers
- instantiate all I/O buffers directly

NGC Project

Differences to the RTL Project:





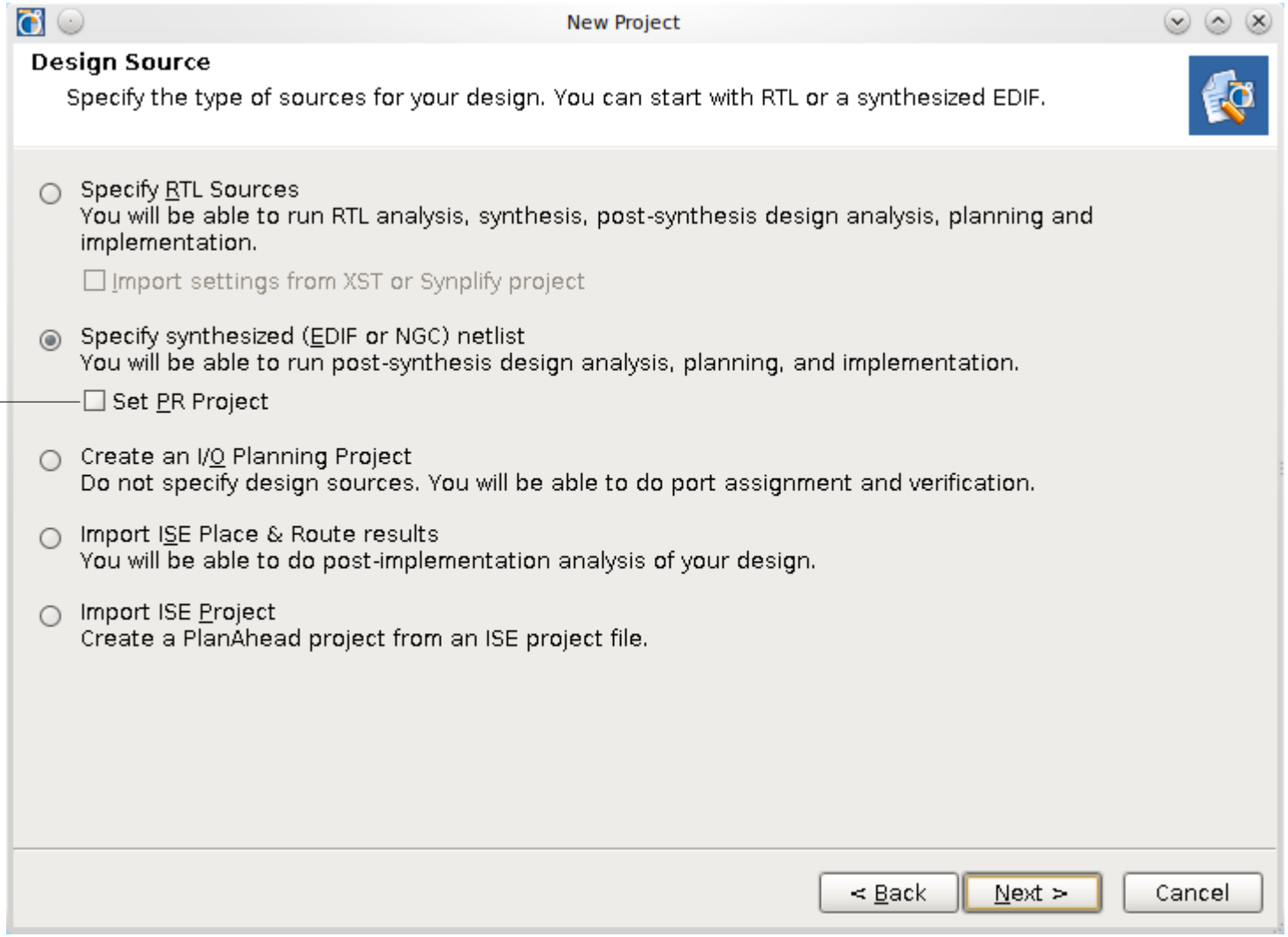
3 Levels of Design Preservation:

- Synthesis (same as Implement)
- Placement
- Routing

Partial Reconfiguration

Requires a special PR-License

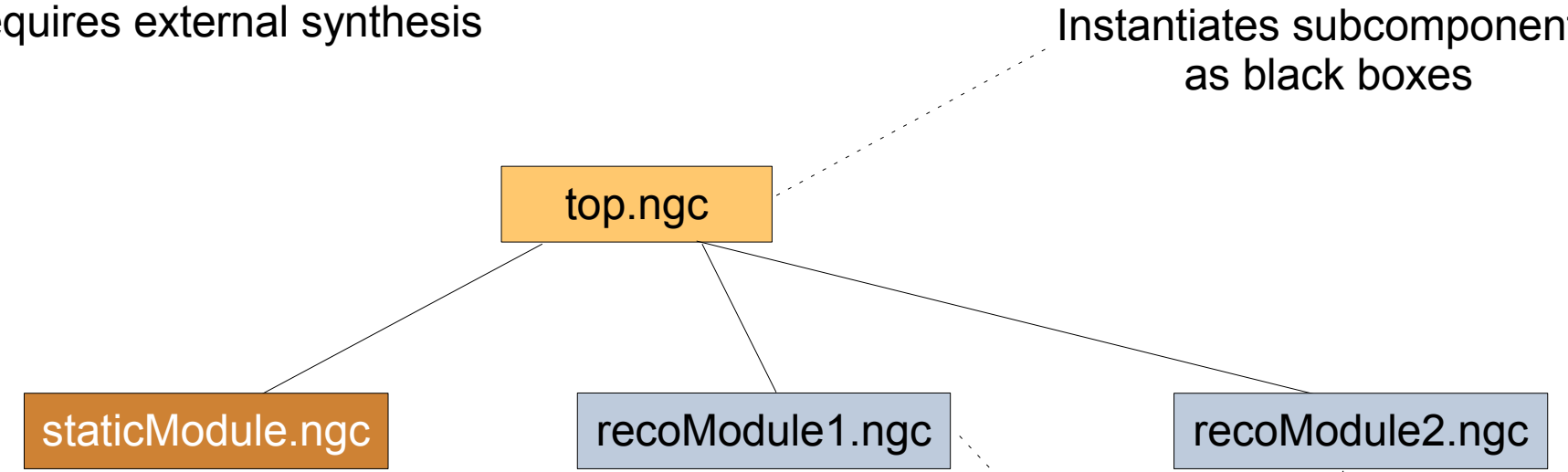
No patches needed any longer!



Partial Reconfiguration

PR designs are NGC designs

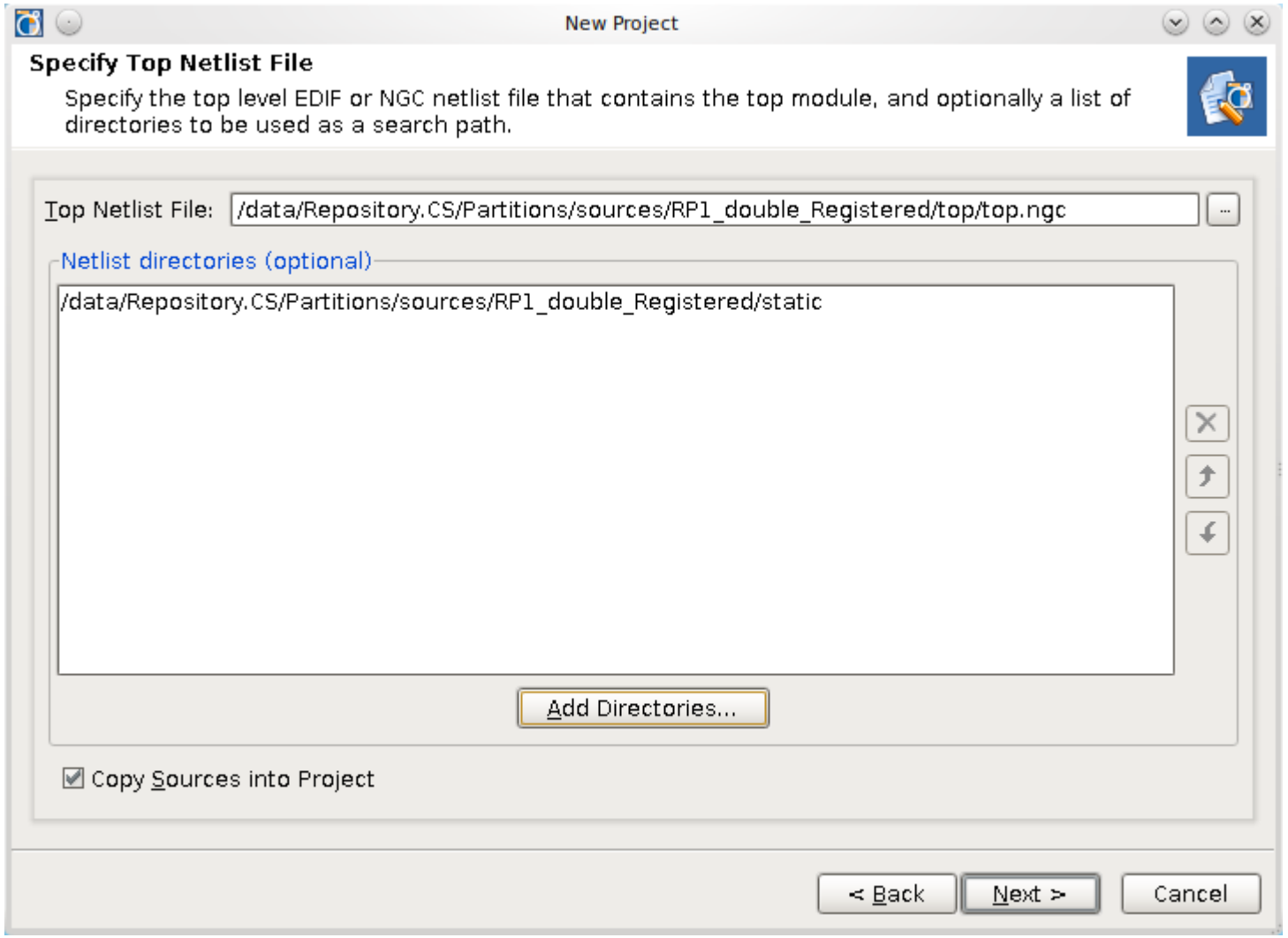
Sources: NGC files (netlists)
==> Requires external synthesis



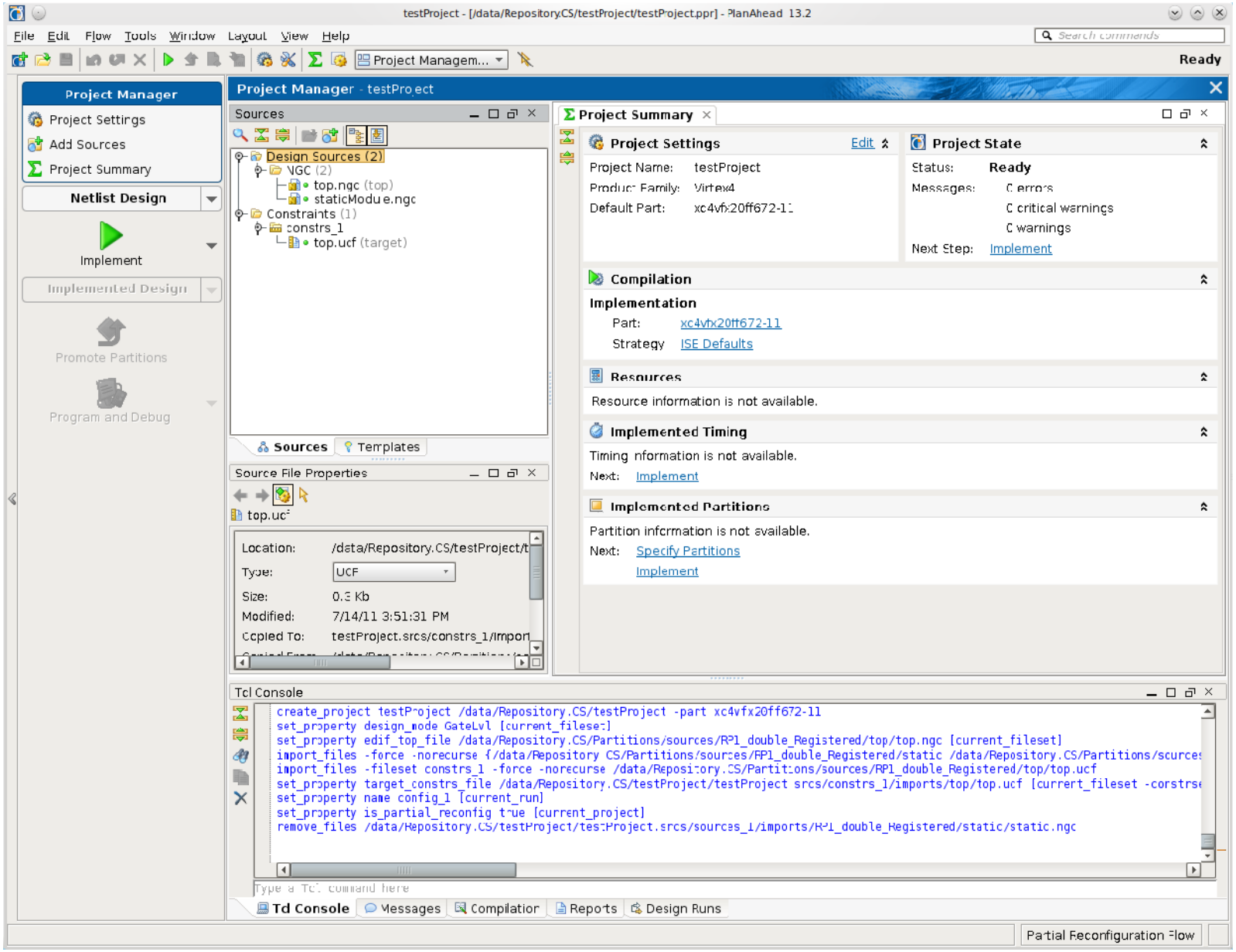
general Synthesis hints:
- deactivate automatically generated I/O buffers
- instantiate all I/O buffers directly

no BUFGs, PLLs,
DCMs, etc. allowed

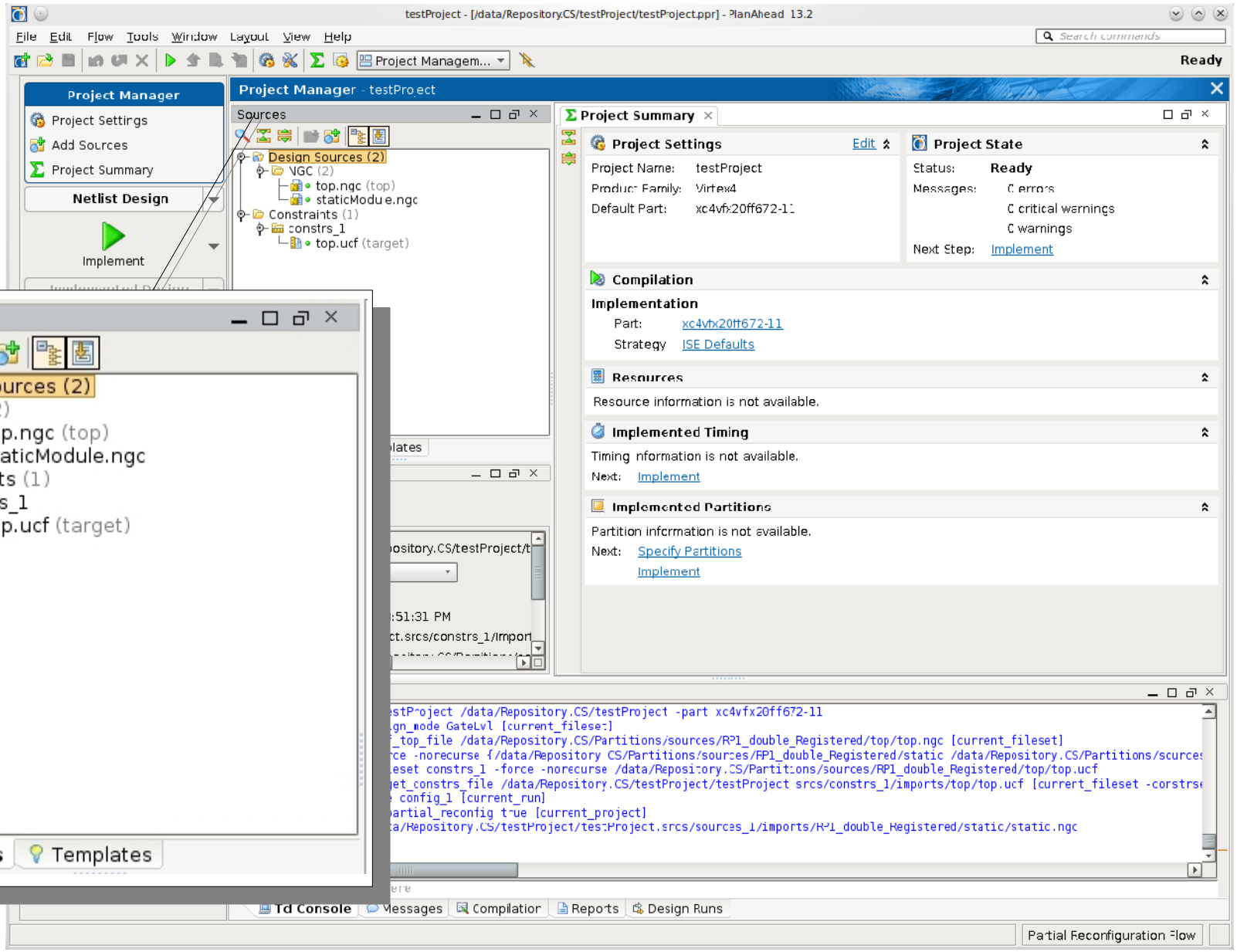
Partial Reconfiguration



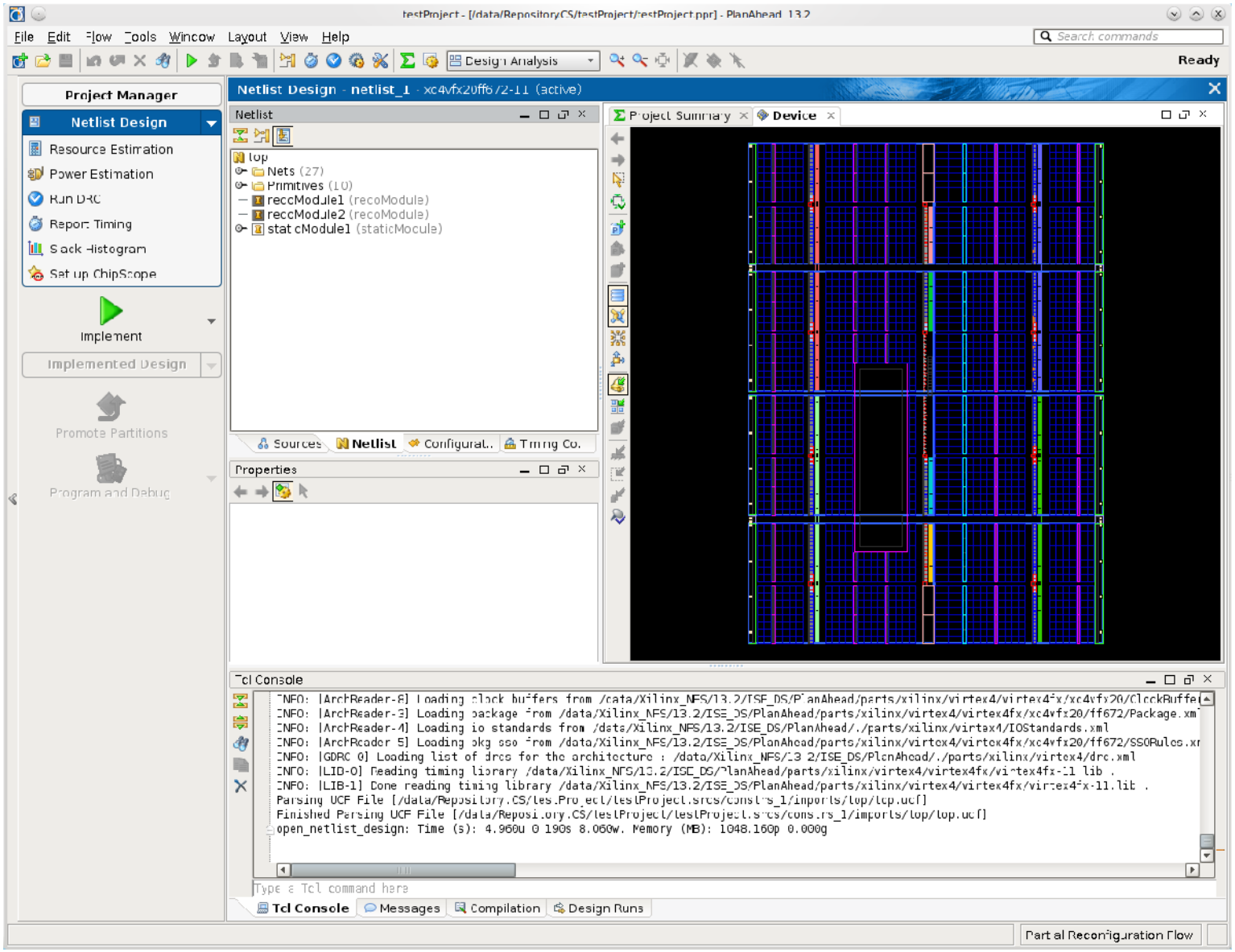
Partial Reconfiguration



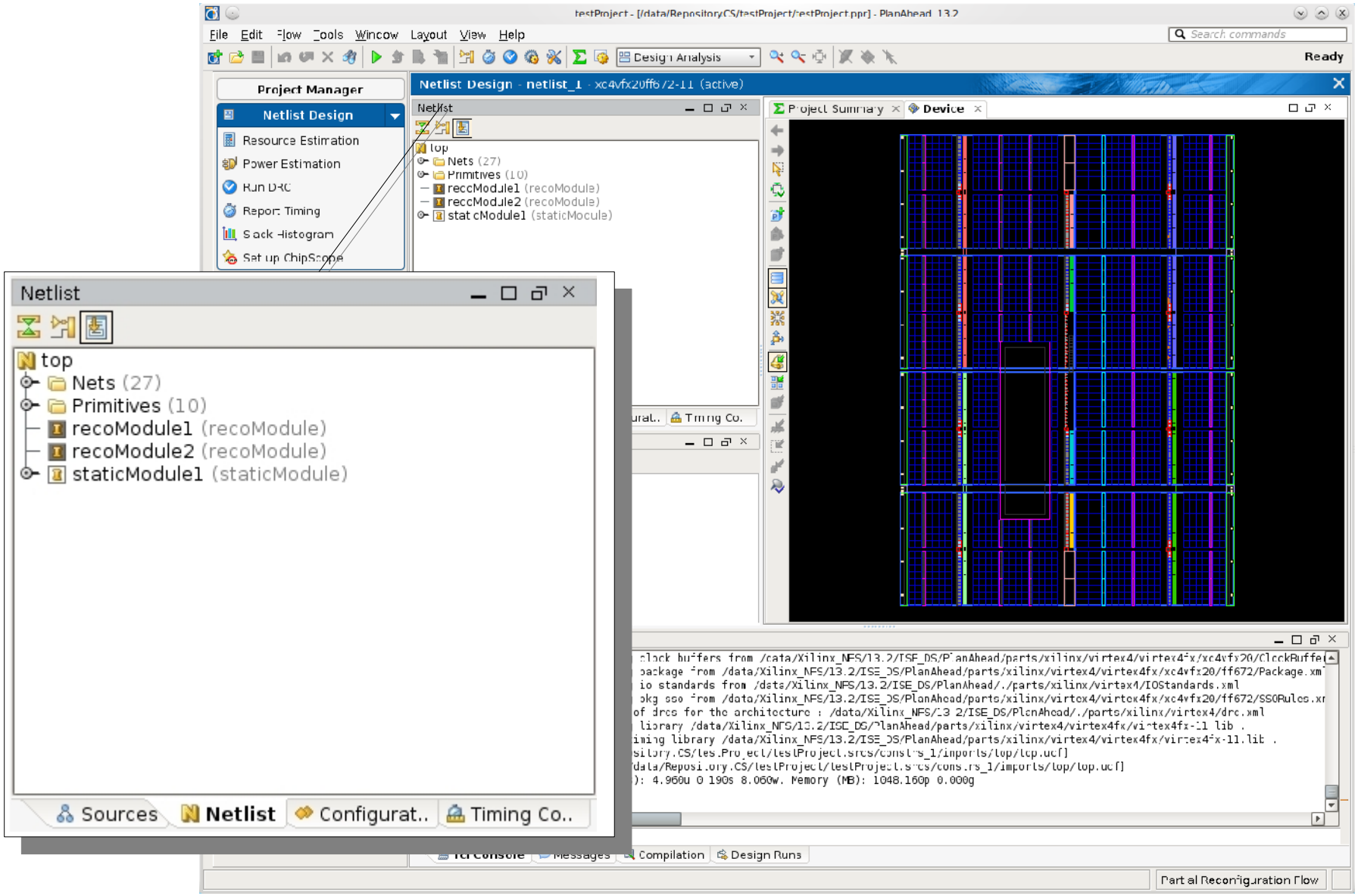
Partial Reconfiguration



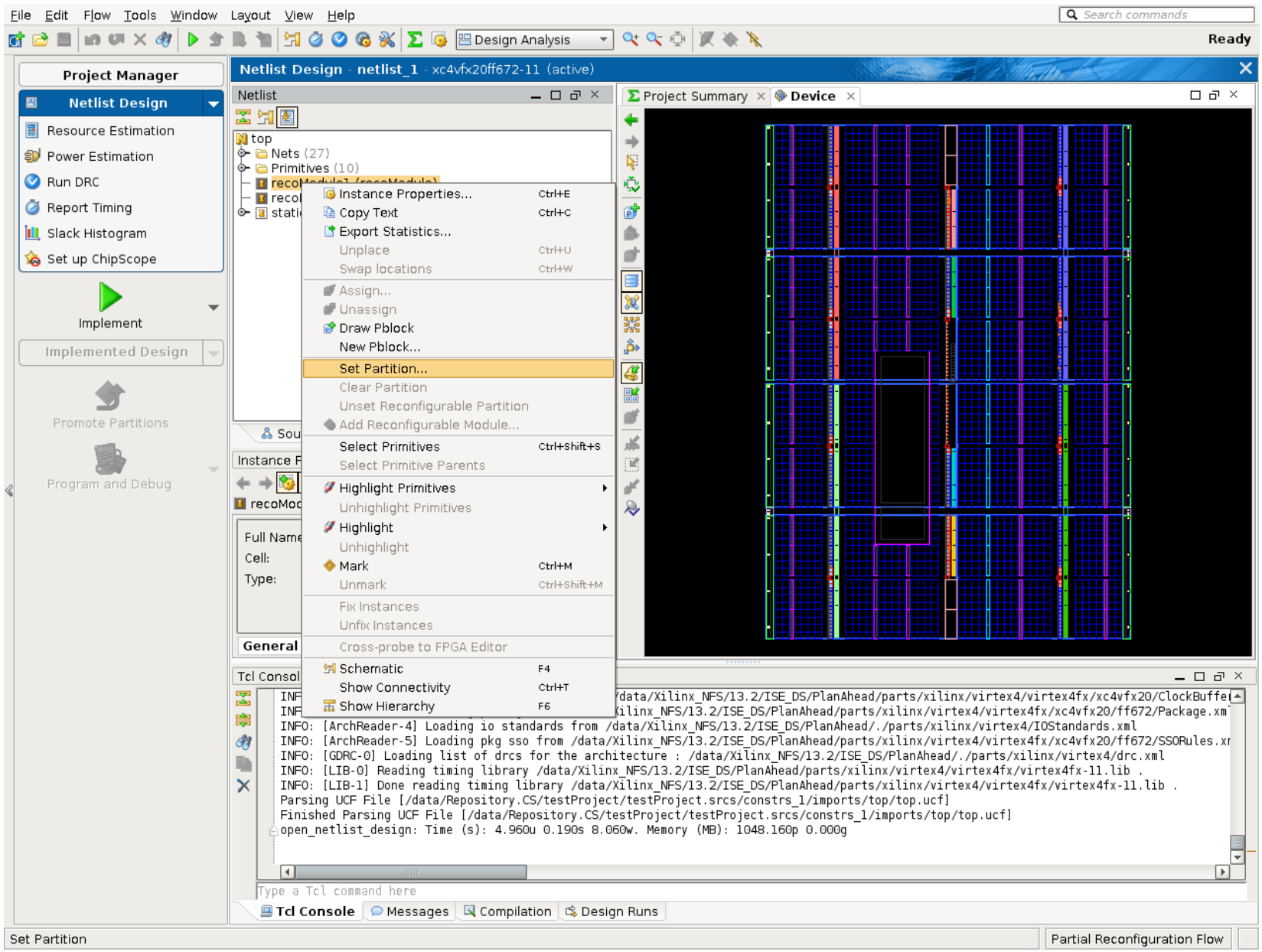
Partial Reconfiguration



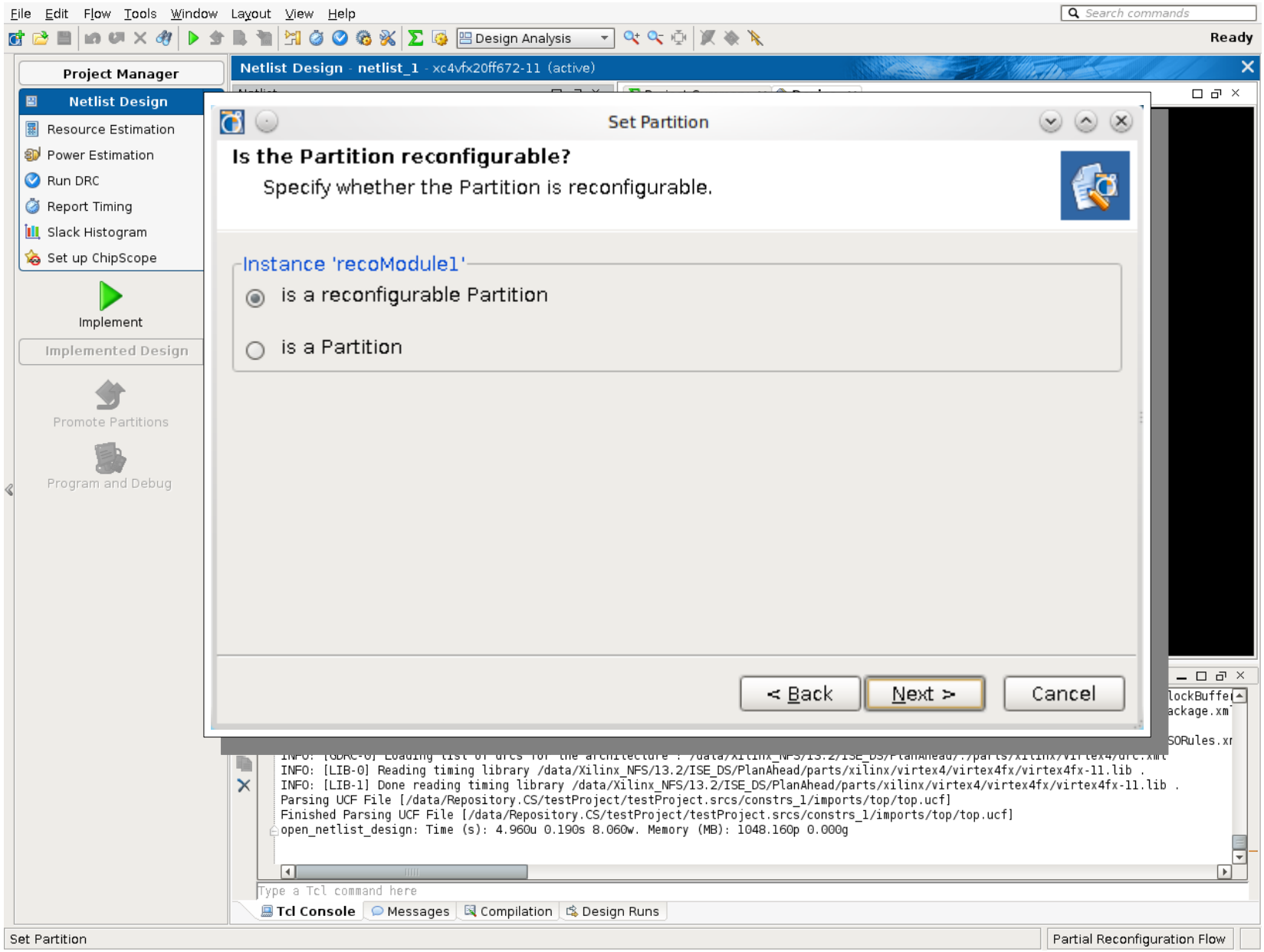
Partial Reconfiguration



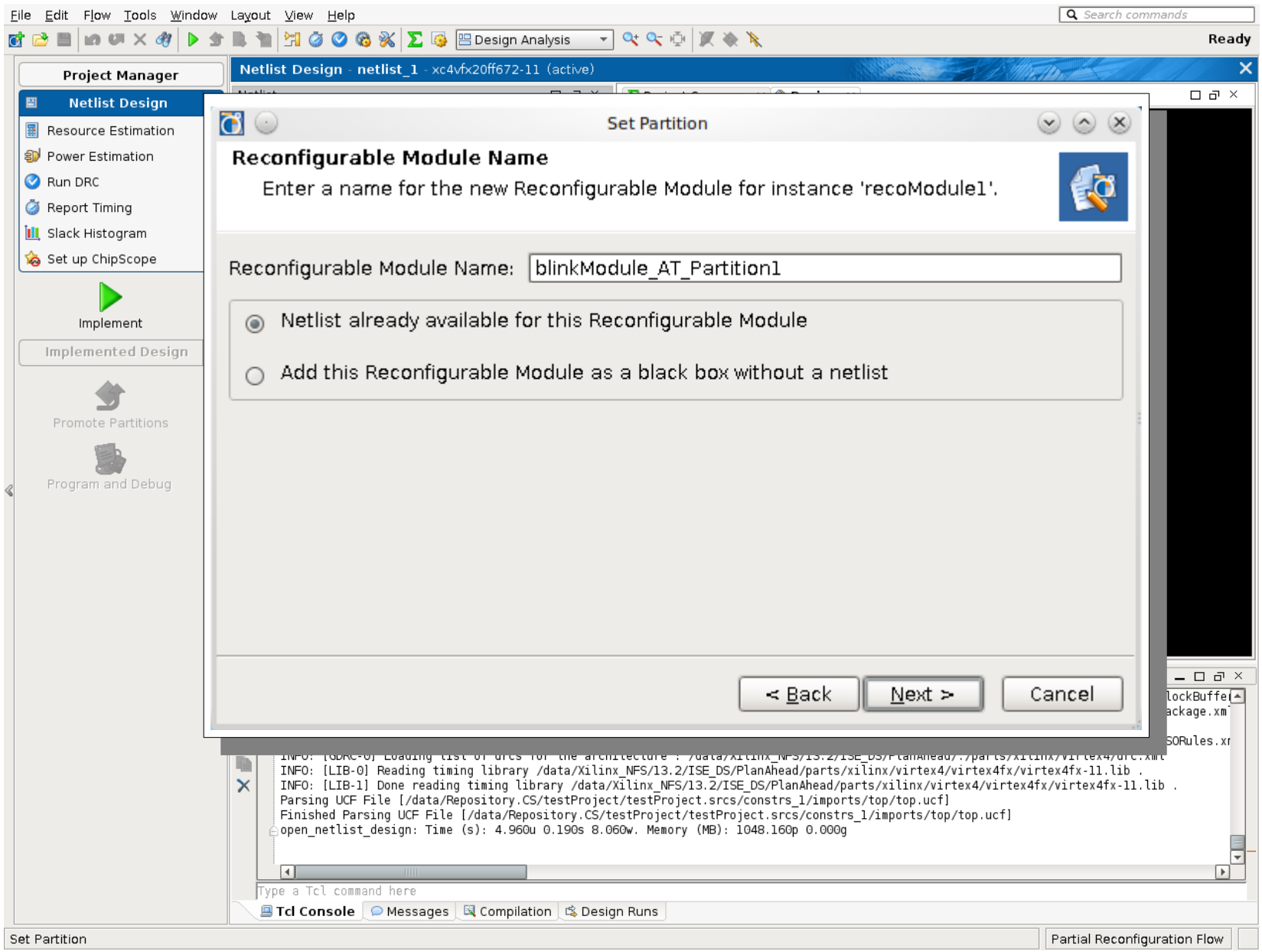
Partial Reconfiguration



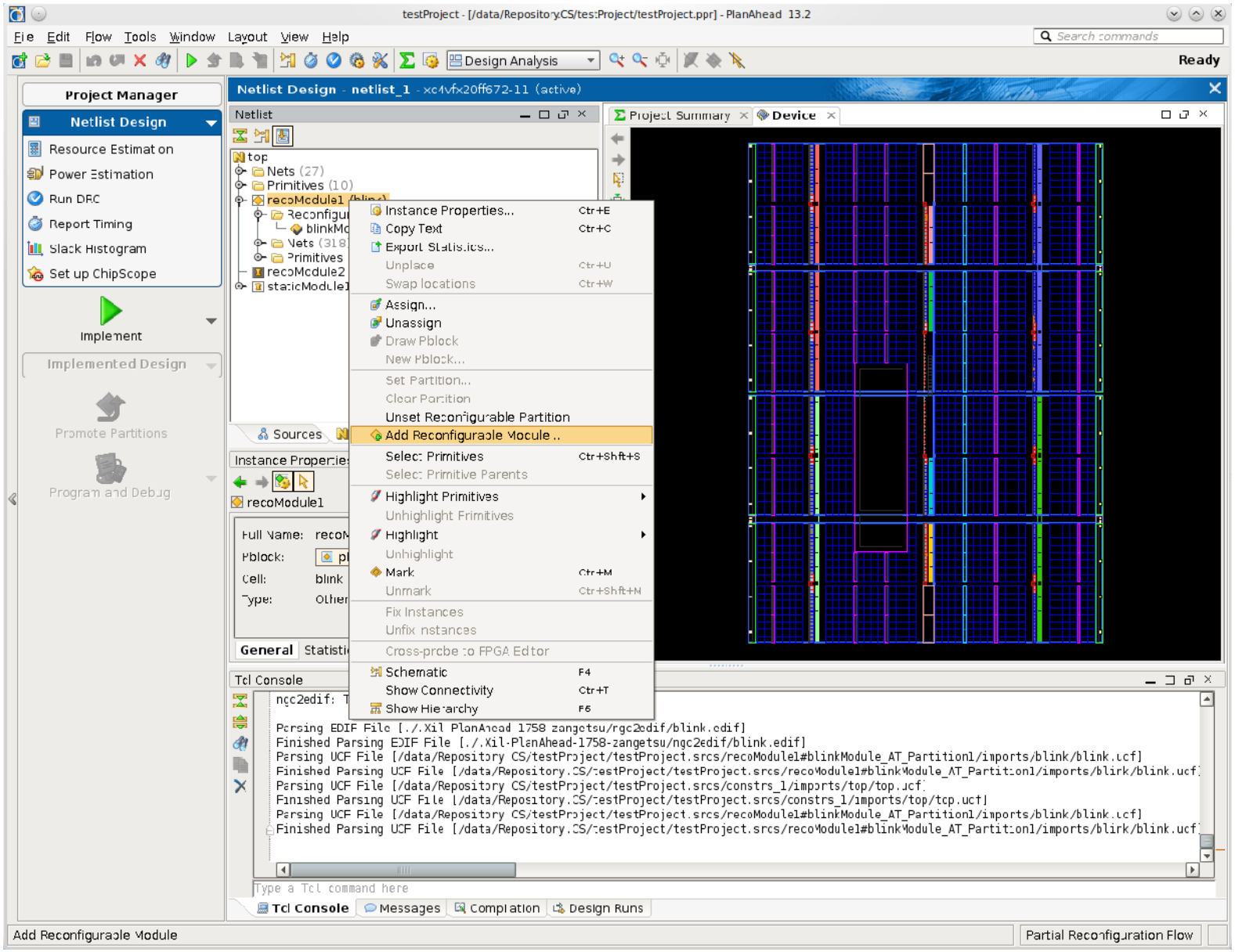
Partial Reconfiguration



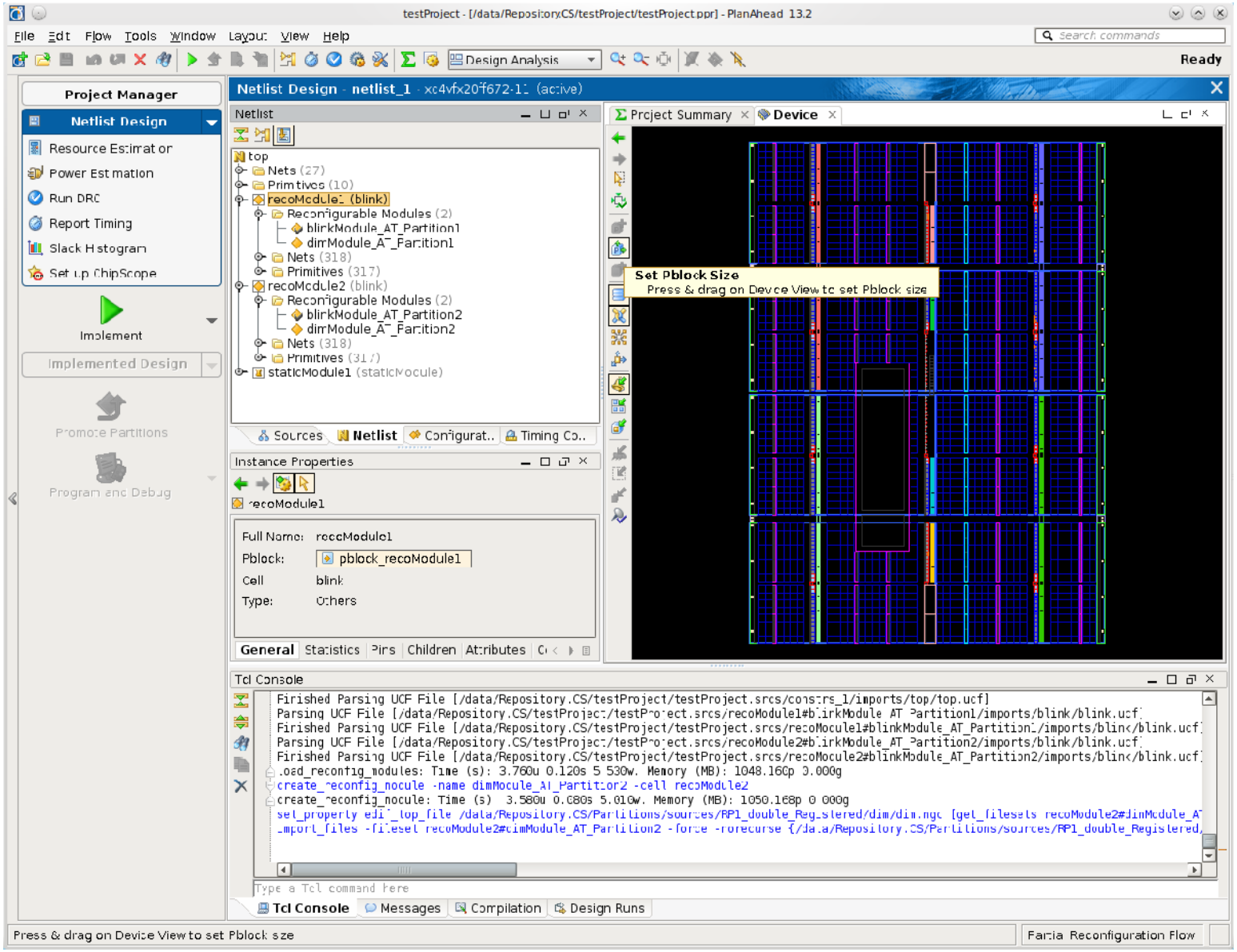
Partial Reconfiguration



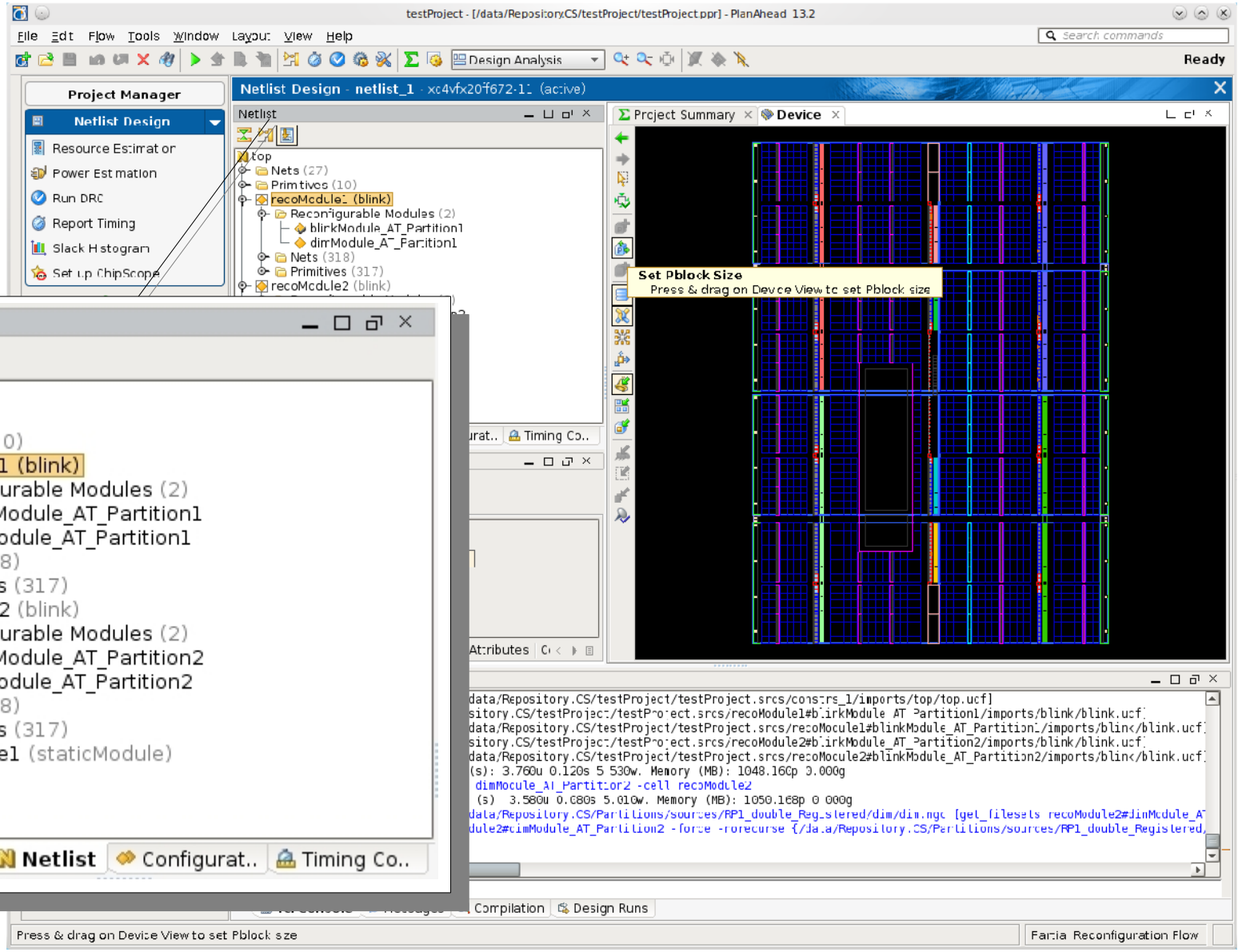
Partial Reconfiguration



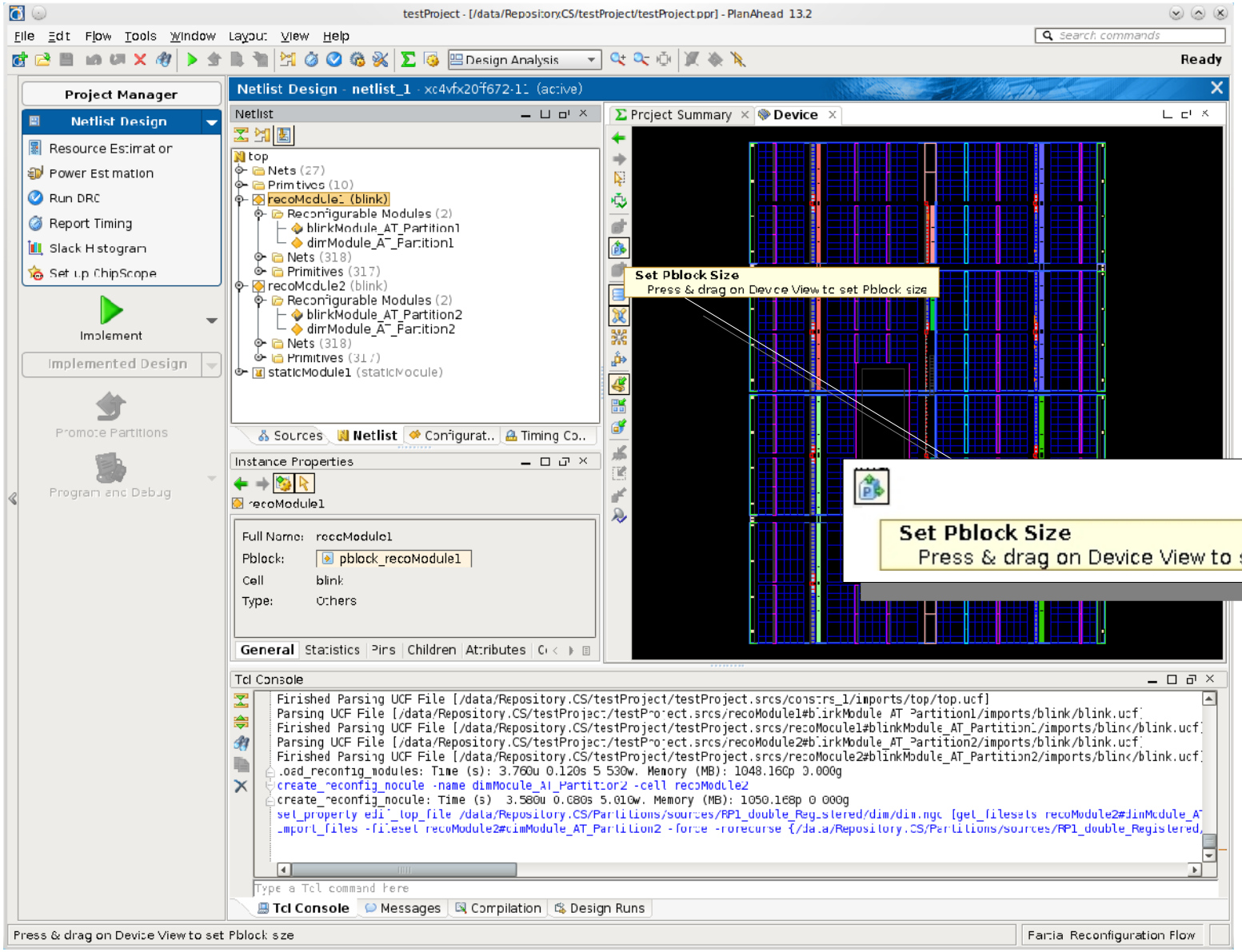
Partial Reconfiguration



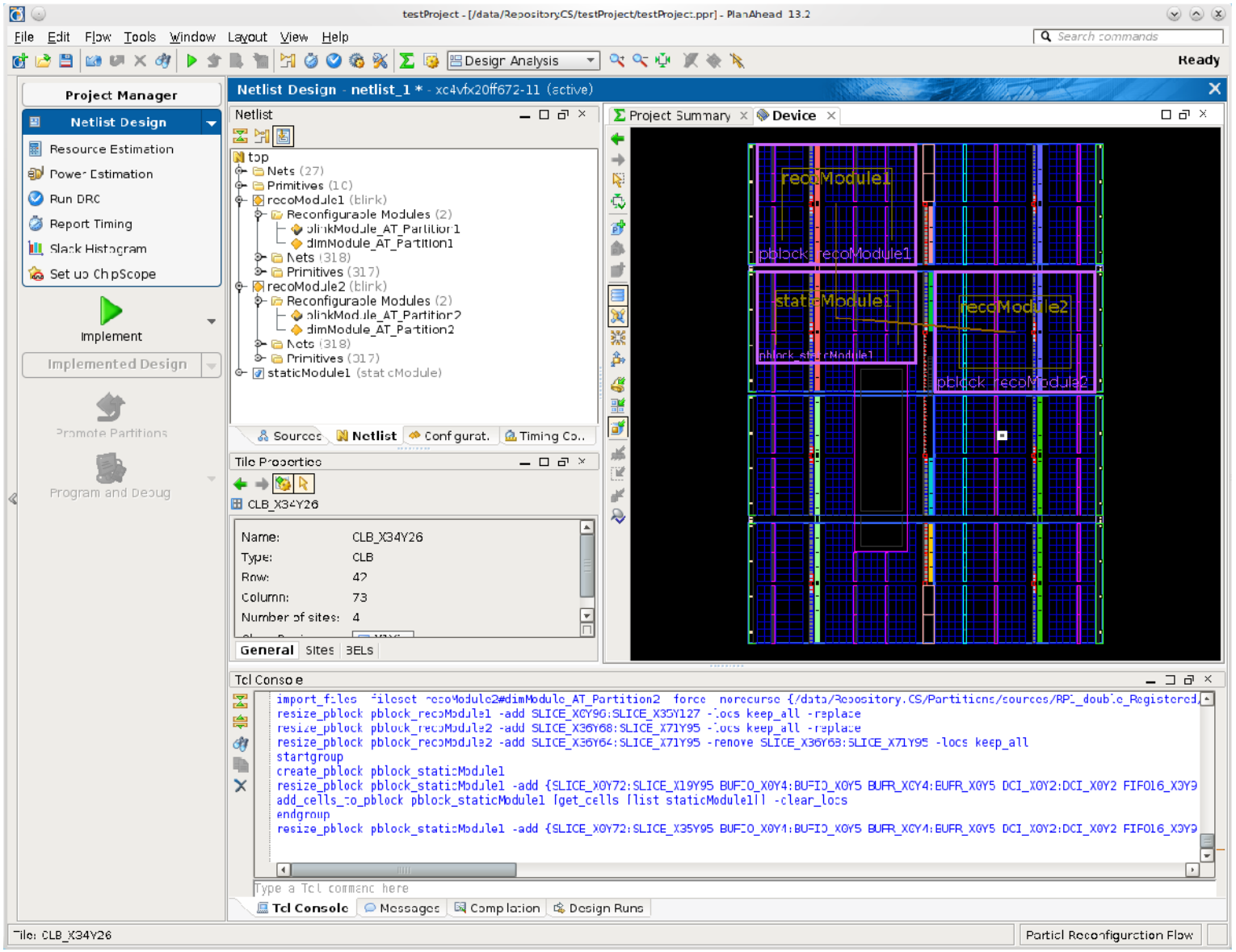
Partial Reconfiguration



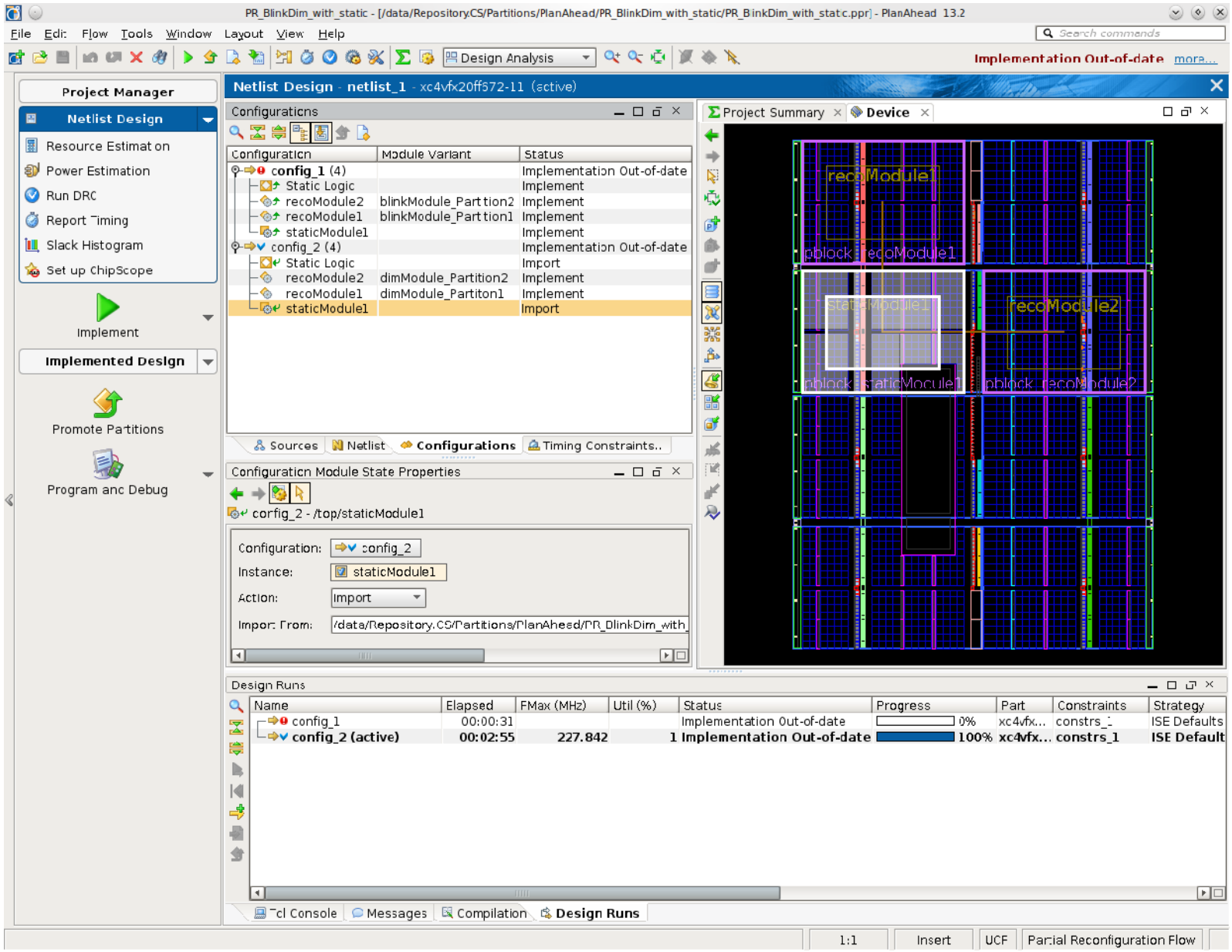
Partial Reconfiguration



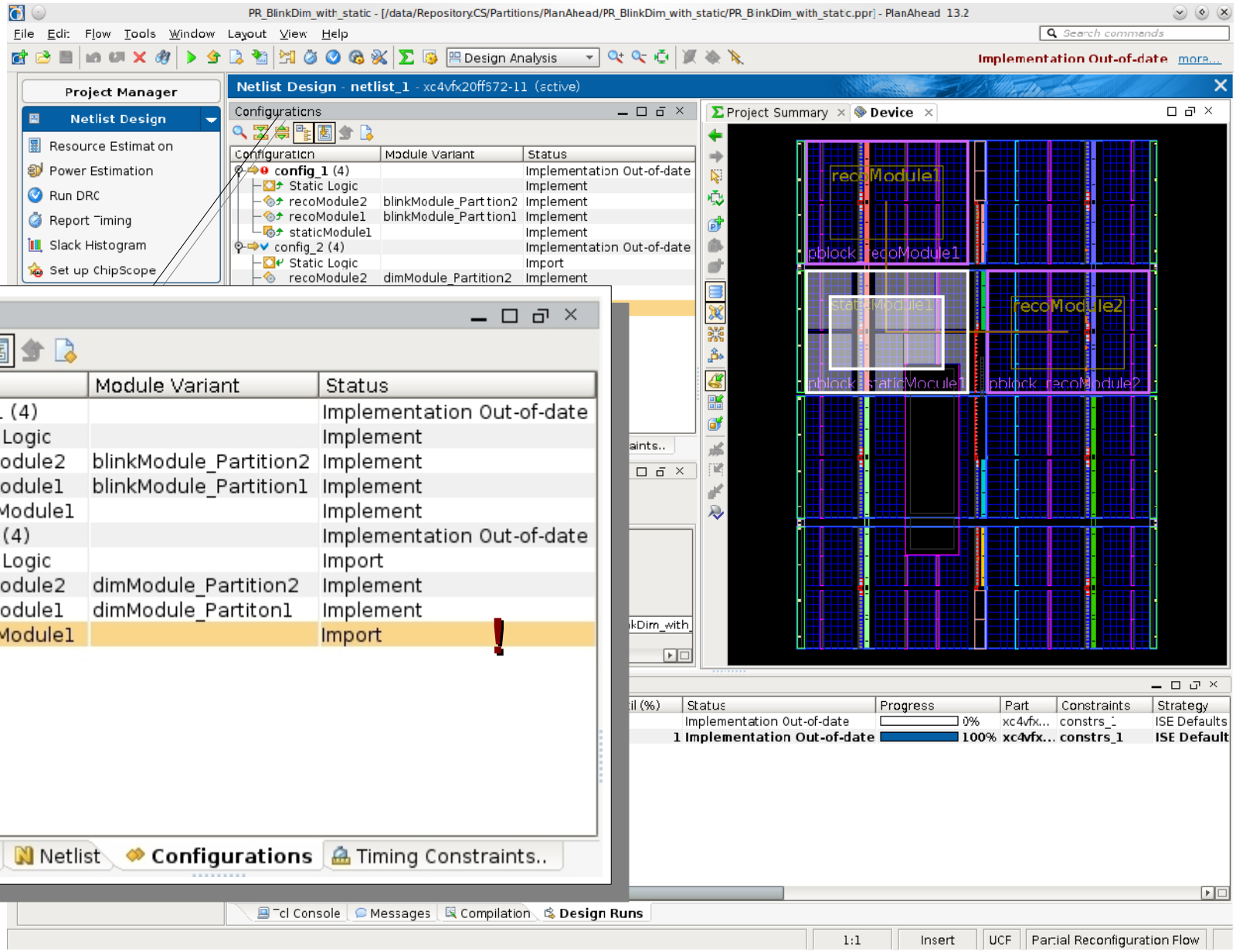
Partial Reconfiguration



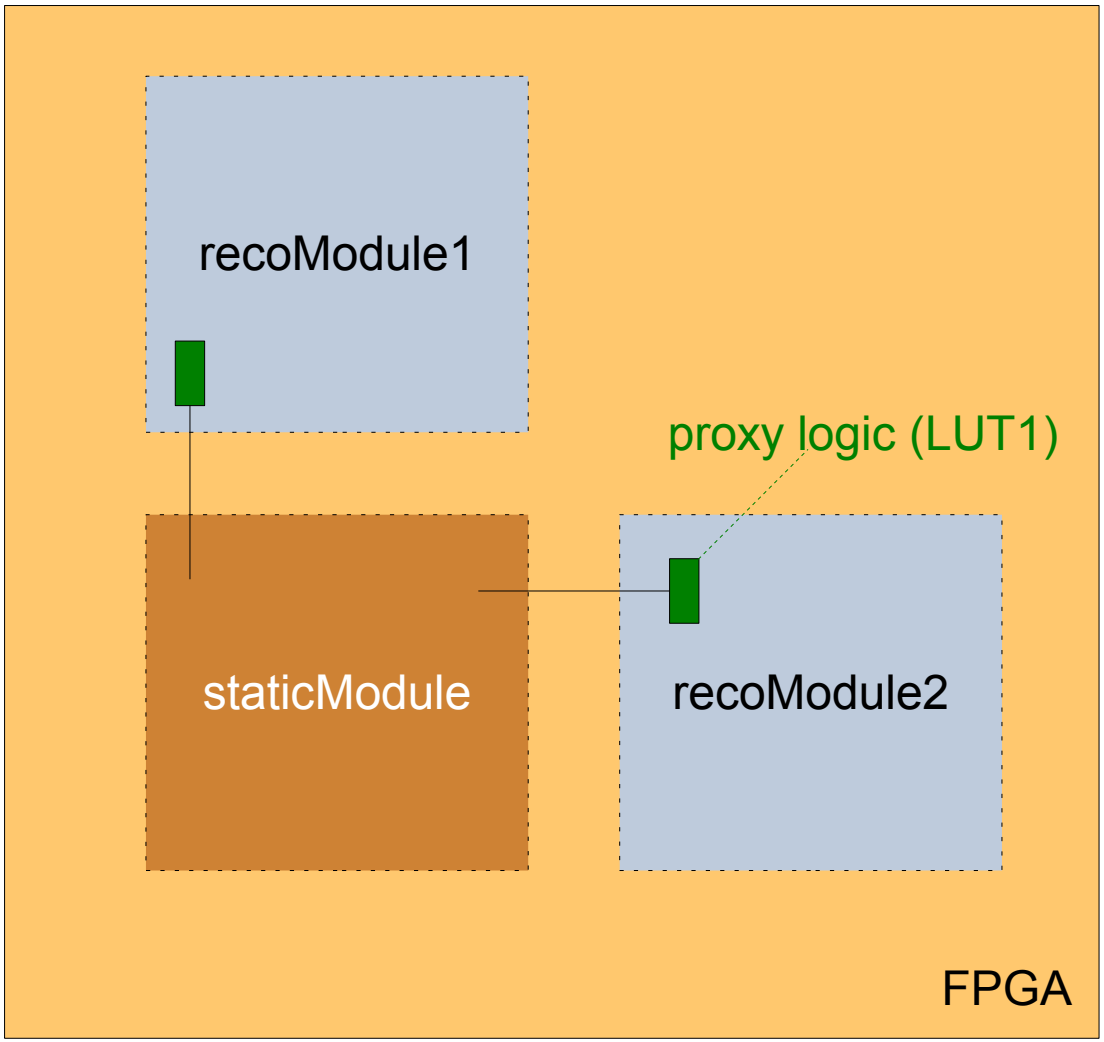
Partial Reconfiguration



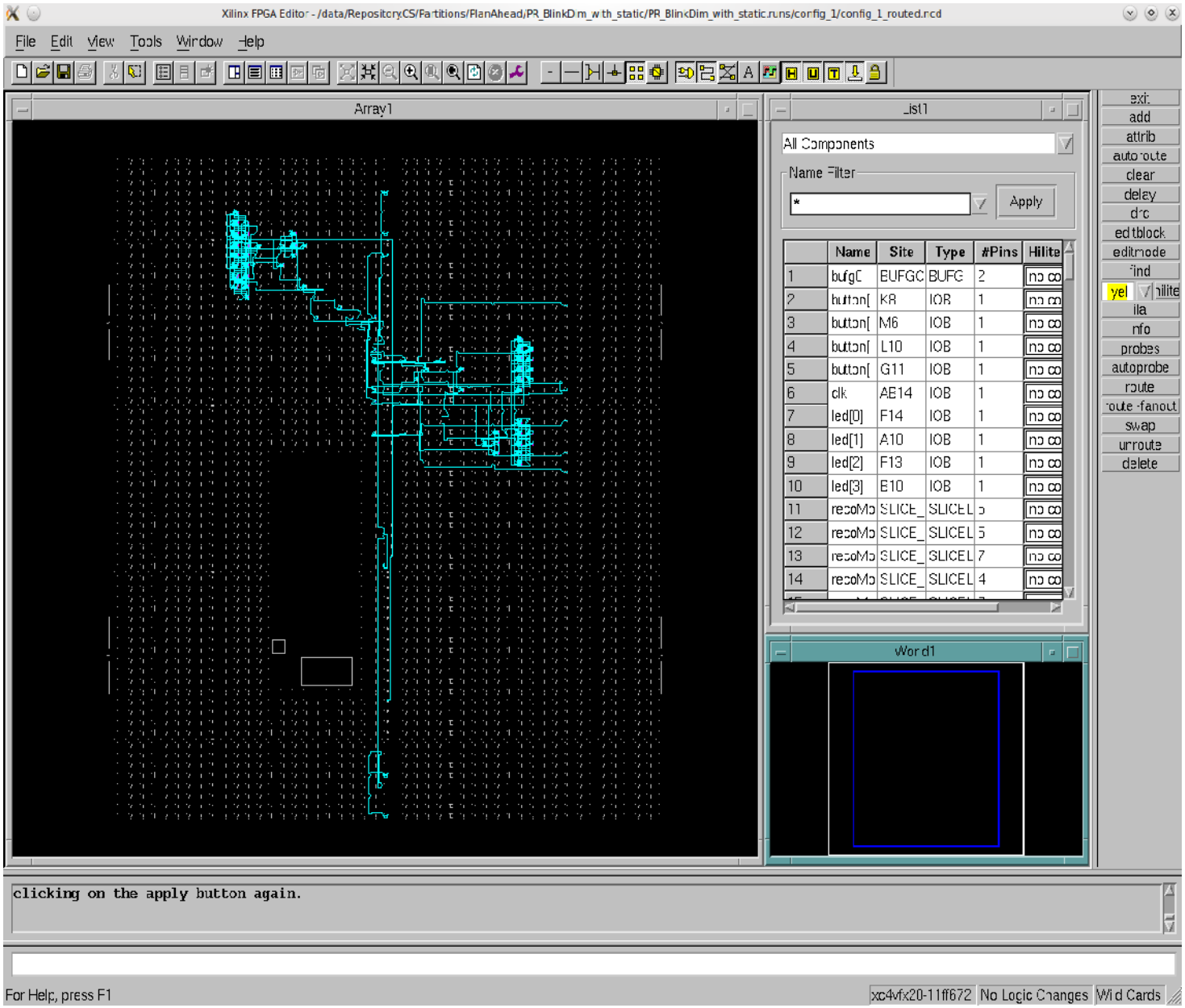
Partial Reconfiguration



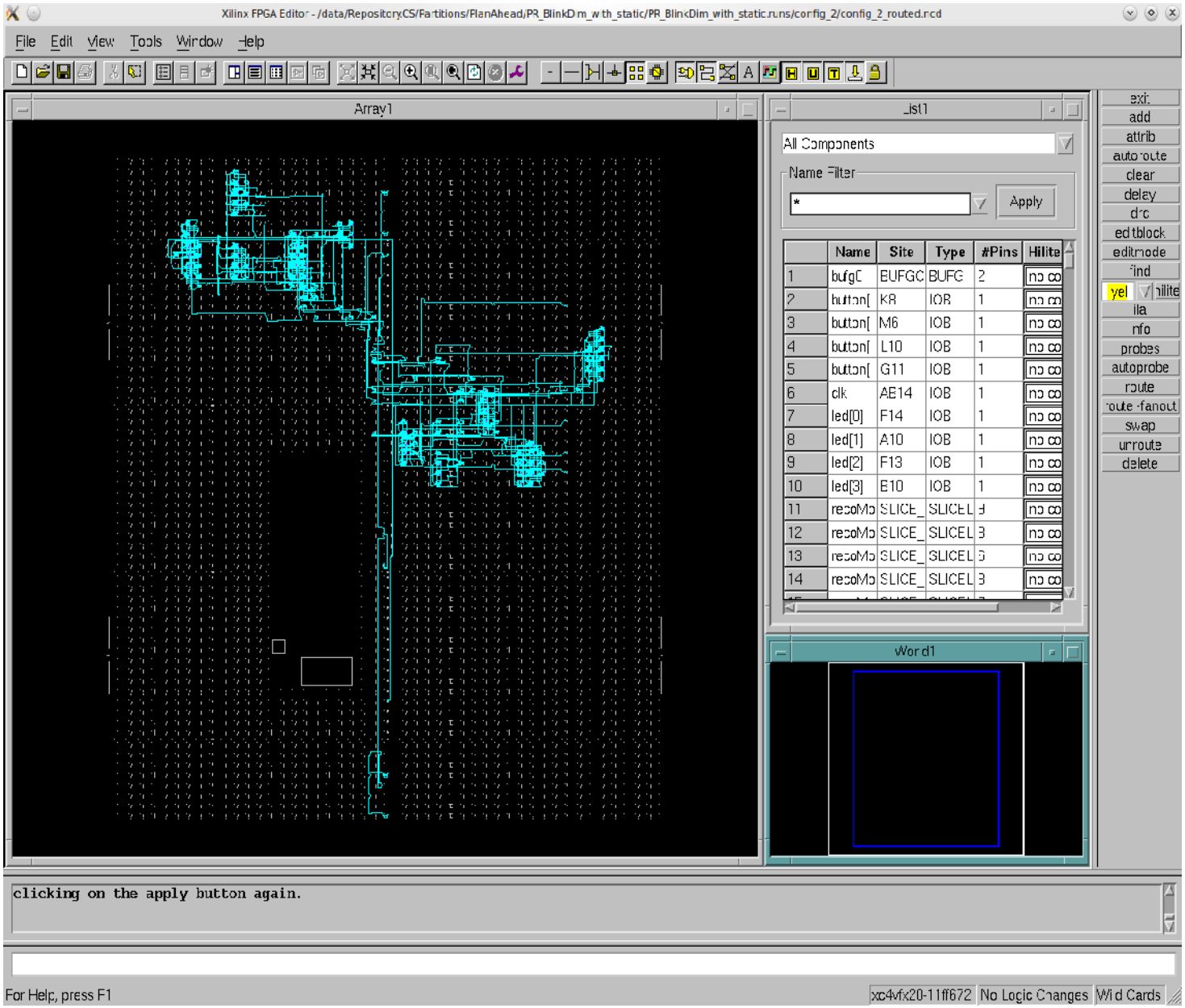
Partial Reconfiguration



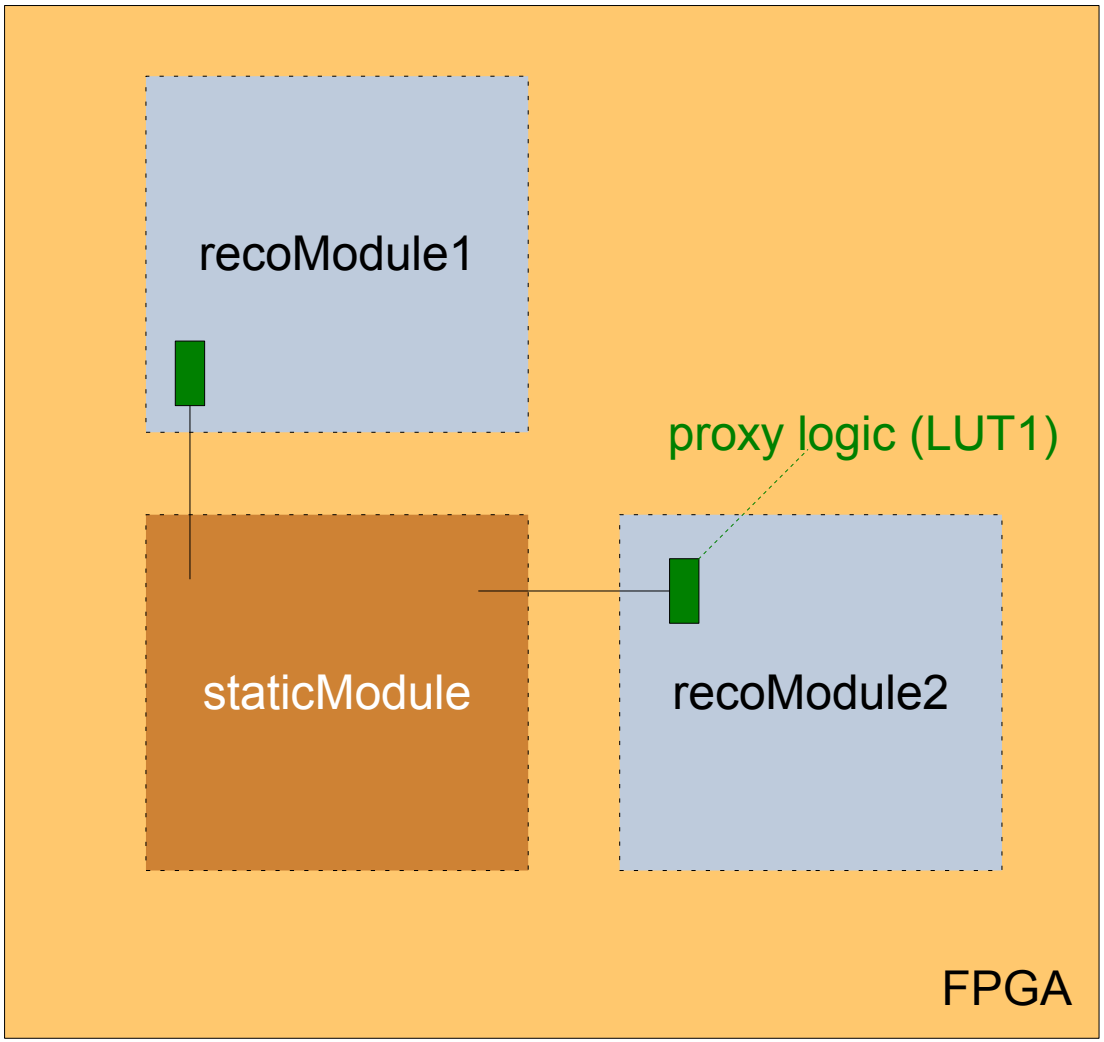
Partial Reconfiguration



Partial Reconfiguration



Conclusion



Problems:
- Timing
- change of **static** Module causes rebuild of **all** Modules
- a Areas using m Modules
  => m configurations
  => m full implementation runs
  => m full bitfiles
  => a • m partial bitfiles
- no support of Spartan-6

Our aims:
- clear Timing
- strict module separation
- movable bitfiles

Questions?