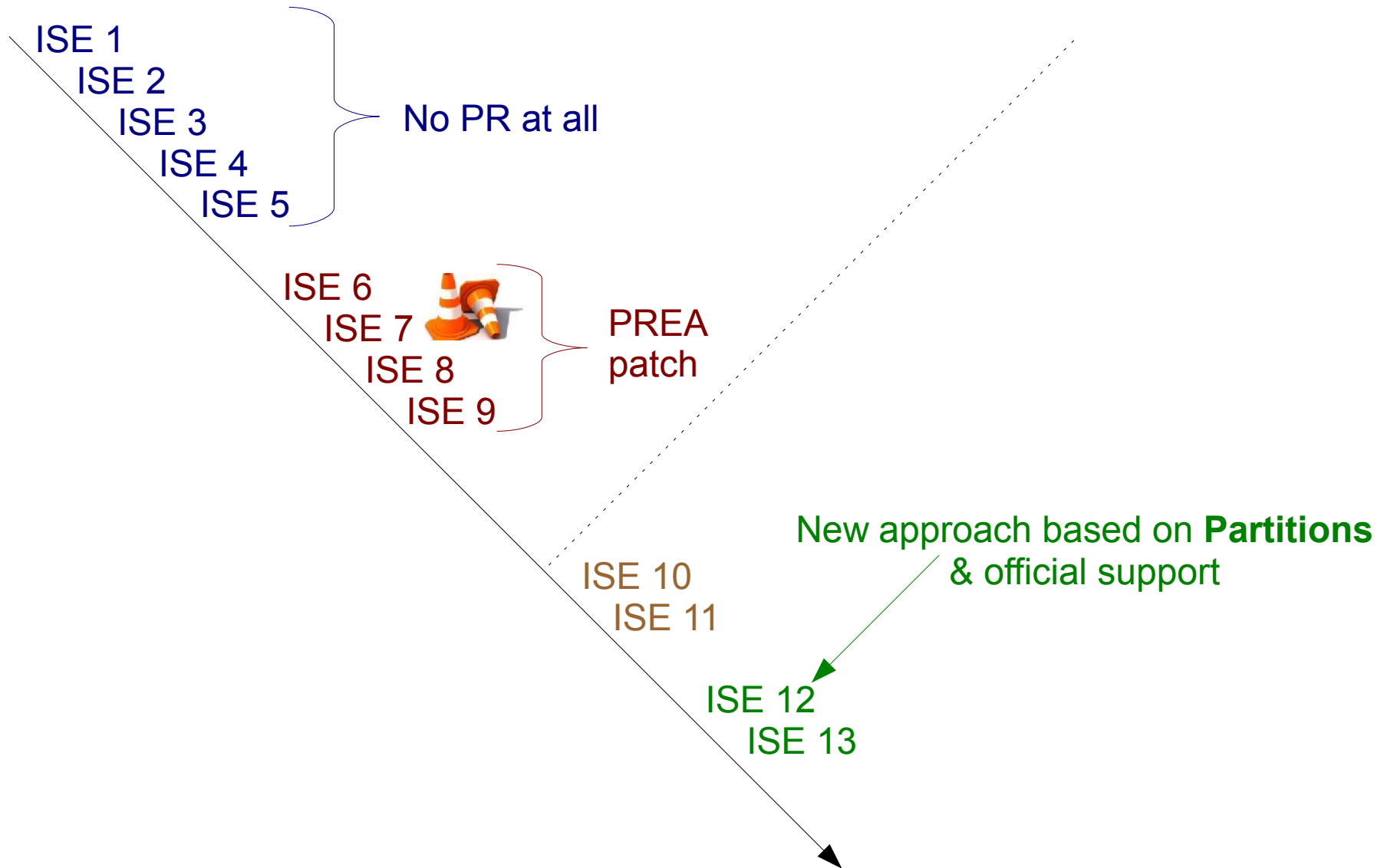


# IRI Frankfurt

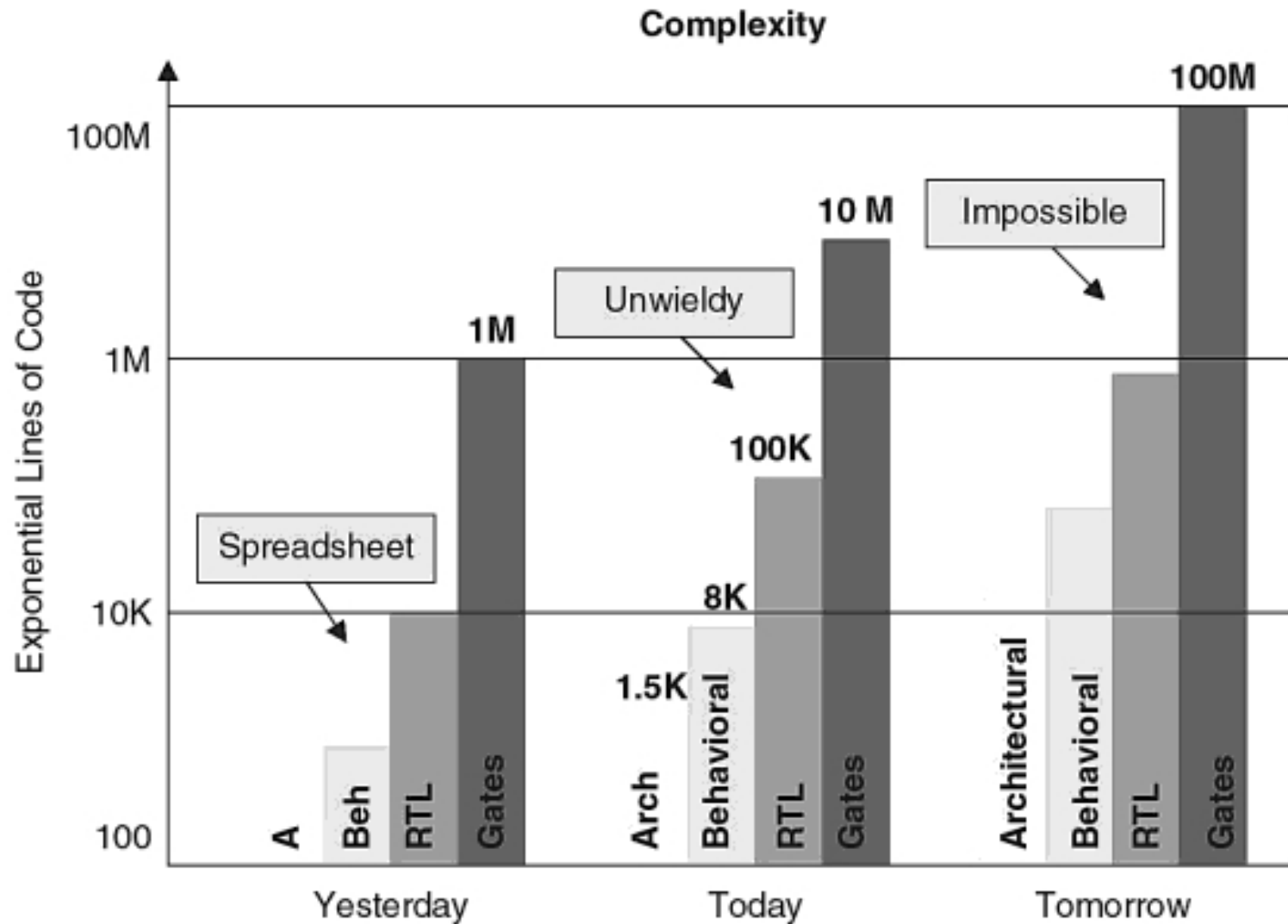
Norbert Abel, Christian Stüllein, Udo Kebschull

***Partitions and Partial Reconfiguration***

# History



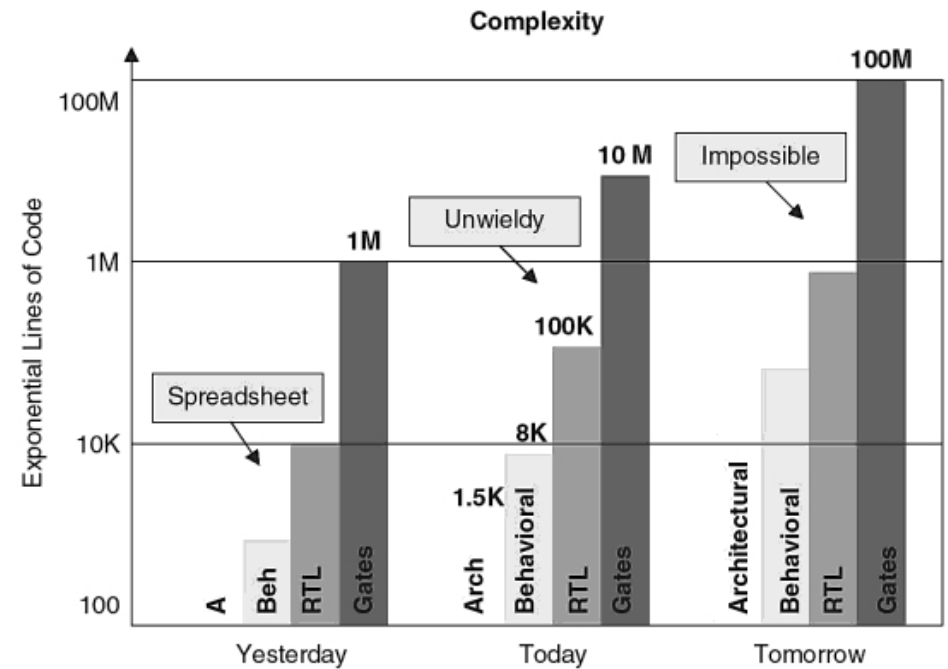
# Motivation



Black, Donovan, Bunton, Keist  
„SystemC: From the Ground Up“

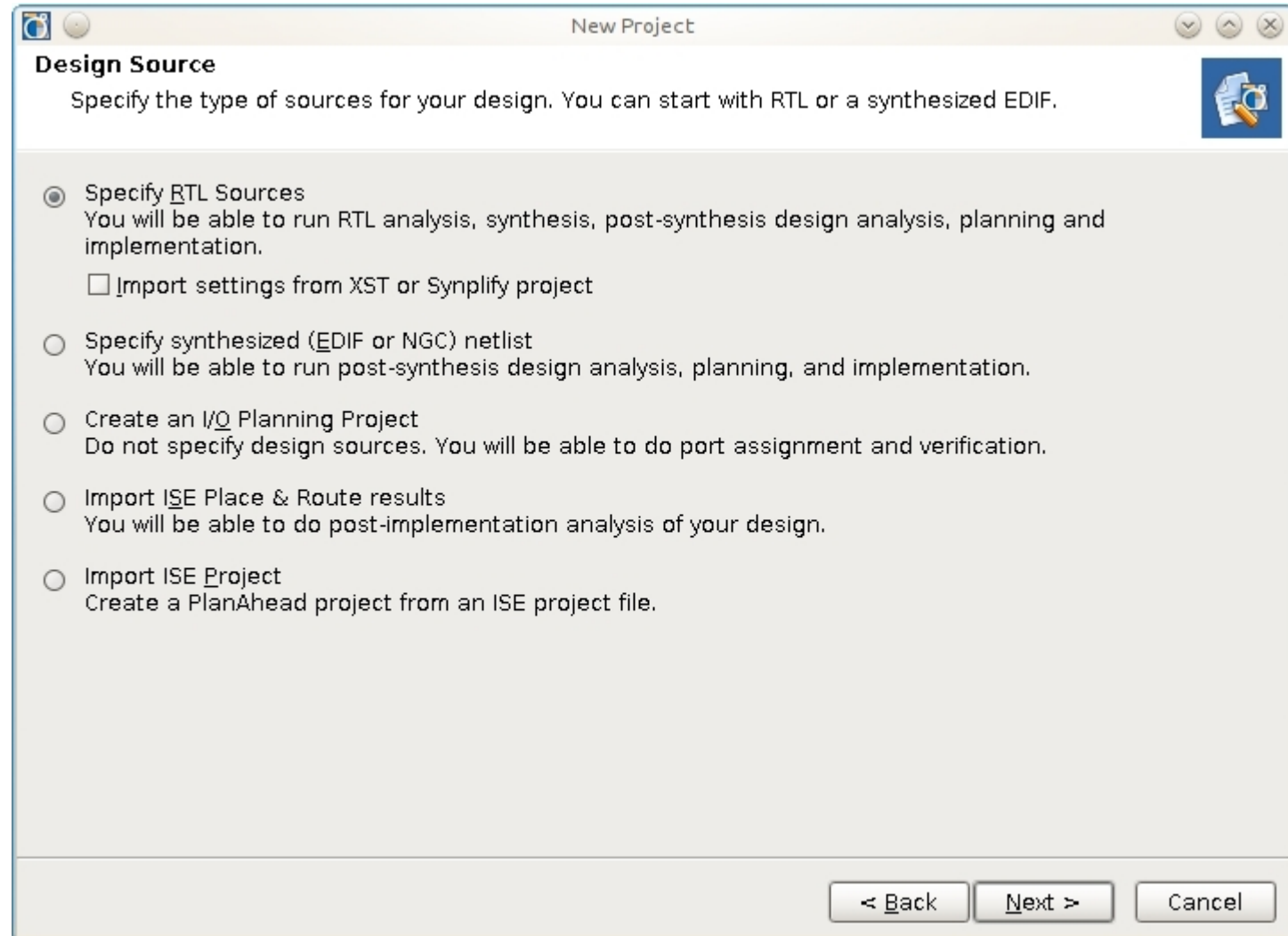
# Motivation

- High Level Synthesis
- Team Design
- Hierarchical Design & Re-Use



# Partitions

Partitions are Xilinx's approach to Team Design and Hierarchical Design  
**Tool: PlanAhead**



# RTL Project

The screenshot displays the Xilinx ISE Project Navigator interface for a project named 'project\_1'. The interface is divided into several panes:

- Project Manager:** Shows the project hierarchy with sources like 'main.vhd' and 'team2.vhd', and constraints like 'main.tcl' and 'team2.tcl'.
- Project Summary:** Provides an overview of the project settings and state.
- Project Settings:** Details the project name, family (FPGA), default part (xc6sl150tgg900-3), and target module name (main).
- Project State:** Indicates the current state as 'Synthesis & Implementation Out-of-date' with 0 errors, 0 critical warnings, and 0 warnings. The next step is 'Synthesis'.
- Compilation:** Compares synthesis and implementation parameters:
  - Synthesis:** Part: xc6sl150tgg900-3, Strategy: PlanAhead Defaults, LUT: 0.0%, -Map: 443.292 MHz.
  - Implementation:** Part: xc6sl150tgg900-3, Strategy: ISE Defaults, LUT: 1.0%, -Map: 502.765 MHz, Timing Score: 0, Unrouted: 0.
- Resources:** A bar chart showing implemented utilization for various resources:

Resource	Utilization (%)
Register	1%
_LUT	1%
Slice	1%
I/O	1%
BUFG	6%
- Implemented Timing:** Shows that all constraints were met, with a minimum period of 1.985 ns and a maximum frequency of 502.765 MHz.
- Implemented Partitions:** Shows the partitioning for the 'main' module on the 'team1\_inst' device.
- Tcl Console:** Displays the command-line output of the project setup, including source scanning and template parsing.

# RTL Project

The screenshot displays the Xilinx ISE Project Navigator interface for a project named 'project\_1'. The main window shows the 'Project Summary' tab, which is divided into several sections:

- Project Settings:** Project Name: project\_1, Prod. of Family: fpga-m6, Default Part: xc6sk150tgg900-3, To: Module Name: main.
- Project State:** Status: Synthesis & Implementation Out-of-date, Messages: 0 errors, 0 critical warnings, 0 warnings, Next Step: Synthesize, Implement.
- Compilation:** Synthesis: Part: xc6sk150tgg900-3, Strategy: PlanAhead Defaults, LUT: 0.0%, -Map: 443.292 MHz; Implementation: Part: xc6sk150tgg900-3, Strategy: ISE Defaults, LUT: 1.0%, -Map: 502.765 MHz, Timing Score: 0, Unrouted: 0.
- Resources:** A bar chart showing Utilization (%) for various resources: Register (1%), LUT (1%), Slice (1%), IO (1%), and BUFG (6%).
- Implemented Timing:** All constraints were met, Minimum Period: 1.985 ns, Maximum Frequency: 502.765 MHz.
- Implemented Partitions:** main, team1\_inst.

The 'Sources' window on the left shows the project's file structure:

- Design Sources (3)
  - VHDL (3)
    - work (3)
      - main.vhd
      - team1.vhd
      - team2.vhd

- Constraints (1)
- constrs\_1
  - main.ucf (target)
  - team1.ucf
  - team2.ucf

The bottom window shows the command line output for the implementation process, including paths to the ISE installation directory and the specific files used for synthesis and implementation.

# RTL Project

Project Manager project\_1

Project Settings

Project Name: project\_1  
Product Family: fpga-a6  
Default Part: xc6sk150tgg900-3  
Top Module Name: main

Project State

Status: **Synthesis & Implementation Out-of-date**  
Messages: 0 errors  
0 critical warnings  
0 warnings  
Next Step: [Synthesize](#)  
[Implement](#)

Compilation

Synthesis

Part: xc6sk150tgg900-3  
Strategy: PlanAhead Defaults

Implementation

Part: xc6sk150tgg900-3  
Strategy: ISE Defaults

```
clkbufds: ibufgds port map (O=>clk, I=>clk_p, IB=>clk_n);  
team1_inst: team1 port map (clk=>clk, led=>led1);  
team2_inst: team2 port map (clk=>clk, led=>led2);
```

Resource Utilization

Utilization (%)

Implemented Timing

All constraints were met.  
Minimum Period: 1.985 ns  
Maximum Frequency: 507.765 MHz  
Go To: [Implemented Design](#)

Implemented Partitions

main team1\_inst

Reports Design Runs



# RTL Project

project\_1 - [C:\e\Repository\hierarchie\project\_1\project\_1\_top] - PlanAhead 13.2

Project Manager project\_1

Project Settings

Project Name: project\_1  
Product Family: fpga-6  
Default Part: xc6sk150tgg900-3  
Top Module Name: main

Project State

Status: **Synthesis & Implementation Out-of-date**  
Messages: 0 errors  
0 critical warnings  
0 warnings  
Next Step: [Synthesize](#)  
[Implement](#)

Compilation

Synthesis	Implementation
Part: xc6sk150tgg900-3	Part: xc6sk150tgg900-3
Strategy: PlanAhead Defaults	Strategy: ISE Defaults
Util: 0.0%	Util: 1.0%

Sources

- Design Sources (3)
  - VHDL (3)
    - work (3)
      - main.vhd
      - team1.vhd
      - team2.vhd
- Constraints (1)
  - constrs\_1
    - main.ucf (target)
    - team1.ucf
    - team2.ucf

```
process (clk)
begin
    if rising_edge(clk) then
        c <= c + 1;
    end if;
end process;

led(3 downto 0) <= c (31 downto 28);
```

# RTL Project

The screenshot displays the ISE Project Navigator interface for a project named 'project\_1'. The 'Sources' window on the left shows a tree structure with 'Design Sources (3)' containing a 'VHDL (3)' folder with 'work (3)' sub-folder containing 'main.vhd', 'team1.vhd', and 'team2.vhd'. Below it is a 'Constraints (1)' folder with 'constrs\_1' containing 'main.ucf (target)', 'team1.ucf', and 'team2.ucf'. The 'Project Summary' window on the right shows 'Project Settings' with 'Project Name: project\_1', 'Product Family: fpga-a6', 'Default Part: xc6sk150tgg900-3', and 'Top Module Name: main'. The 'Project State' window shows 'Status: Synthesis & Implementation Out-of-date', 'Messages: 0 errors', '0 critical warnings', and '0 warnings'. The 'Compilation' window shows 'Synthesis' with 'Part: xc6sk150tgg900-3', 'Strategy: PlanAhead Defaults', 'LUT: 0.0%', and 'Max: 443.292 MHz'. The 'Implementation' window shows 'Part: xc6sk150tgg900-3', 'Strategy: ISE Defaults', 'LUT: 1.0%', and 'Max: 502.762 MHz'. A code snippet is overlaid on the right side of the image, showing a VHDL process:

```
process (clk)
begin
    if rising_edge(clk) then
        c(31 downto 0) <= c(30 downto 0) & c(31);
    end if;
end process;

led(3 downto 0) <= c (31 downto 28);
```

# RTL Project

The screenshot displays the Xilinx ISE Project Navigator interface for a project named 'project\_1'. The interface is divided into several panes:

- Project Manager:** Shows the project hierarchy with 'Sources' and 'Constraints'. The 'Sources' pane lists files like 'main.vhd', 'team1.vhd', and 'team2.vhd'. The 'Constraints' pane shows 'constraints\_1' with files 'main.tdf', 'team1.tcl', and 'team2.tcl'.
- Project Summary:** Contains sub-panels for:
  - Project Settings:** Project Name: project\_1, Product Family: fpga-a6, Default Part: xc6sk150tgg900-3, Top Module Name: main.
  - Project State:** Status: Synthesis & Implementation Out-of-date, Messages: 0 errors, 0 critical warnings, 0 warnings. Next Step: Synthesize, Implement.
  - Compilation:** Synthesis: Part: xc6sk150tgg900-3, Strategy: PlanAhead Defaults, LUT: 0.0%, -Map: 443.292 MHz. Implementation: Part: xc6sk150tgg900-3, Strategy: ISE Defaults, LUT: 1.0%, -Map: 502.765 MHz, Timing Score: 0, Unrouted: 0.
  - Resources:** A bar chart showing Utilization (%) for various resources: Register (1%), LUT (1%), Slice (1%), I/O (1%), and BUFG (6%).
  - Implemented Timing:** All constraints were met. Minimum Period: 1.985 ns, Maximum Frequency: 502.765 MHz. Go To: Implemented Design.
  - Implemented Partitions:** main, team1\_inst.
- Tcl Console:** Shows the following output:

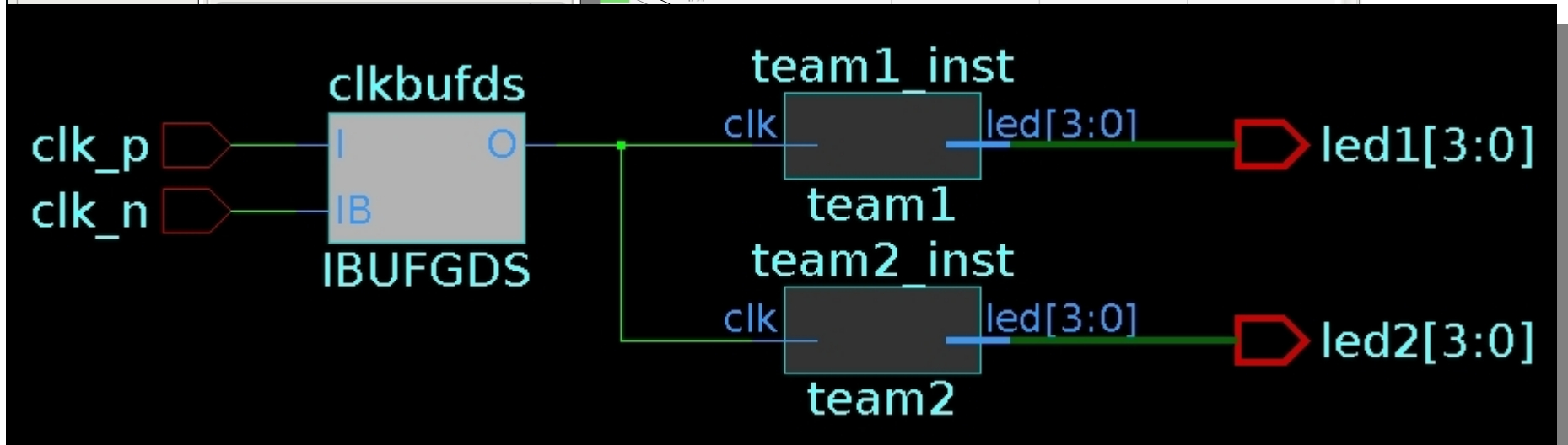
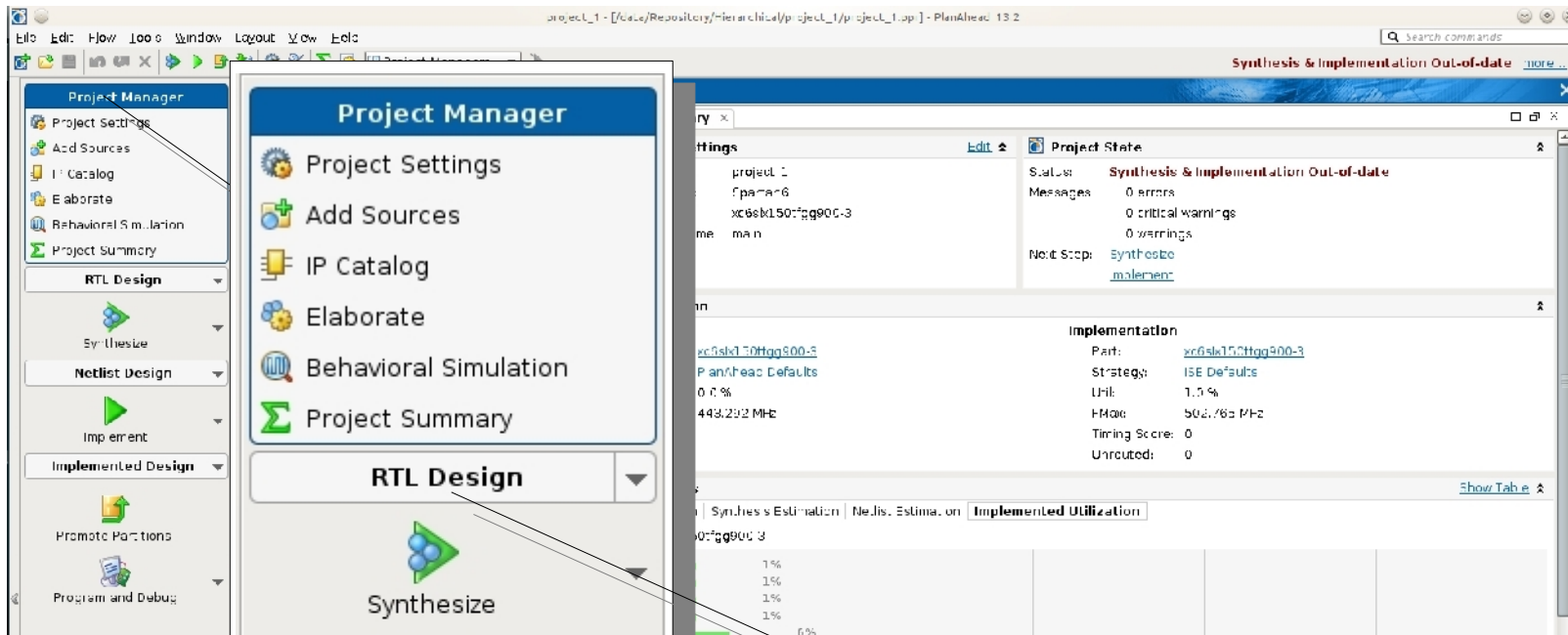
```
INFO: [ProjDB 1] Scanning sources...
INFO: [ProjDB 2] Source scan complete
INFO: [Project-1] Project 'project_1.ppr' upgraded for this version of PlanAhead.
Parsing template file /data/Xilinx/NFS/13.2/ISE_DS/ISE/data/projects/templates/verilog.xml.
Finished parsing template file /data/Xilinx/NFS/13.2/ISE_DS/ISE/data/projects/templates/vhdl.xml.
Parsing template file /data/Xilinx/NFS/13.2/ISE_DS/ISE/data/projects/templates/vhdl.xml.
Finished parsing template file /data/Xilinx/NFS/13.2/ISE_DS/ISE/data/projects/templates/vhdl.xml.
Parsing template file /data/Xilinx/NFS/13.2/ISE_DS/ISE/data/projects/templates/ucf.xml.
Finished parsing template file /data/Xilinx/NFS/13.2/ISE_DS/ISE/data/projects/templates/ucf.xml.
```

# RTL Project

The screenshot displays the Xilinx ISE Project Navigator interface. The main window is titled "project\_1 - [C:\xilinx\Repository\hierarchy\project\_1\project\_1\_top] - PlanAhead 13.2". The interface is divided into several panels:

- Project Manager:** A central panel with a blue header. It contains a list of actions: Project Settings, Add Sources, IP Catalog, Elaborate, Behavioral Simulation, and Project Summary. Below this list are four large buttons: "RTL Design" (with a dropdown arrow), "Synthesize" (with a green play button icon), "Netlist Design" (with a dropdown arrow), "Implement" (with a green play button icon), "Implemented Design" (with a dropdown arrow), "Promote Partitions" (with a green arrow icon), and "Program and Debug" (with a green play button icon).
- Project State:** A panel on the right showing the status of the project. It includes a "Status" section with "Messages: 0 errors", "0 critical warnings", and "0 warnings". The "Next Step" is "Synthesize" and "Implement".
- Implemented Utilization:** A bar chart showing the utilization of resources. The x-axis is labeled "Utilization (%)" and ranges from 0 to 100. The y-axis shows utilization percentages for different resources: 1%, 1%, 1%, 1%, and 6%.
- Implemented Timing:** A panel showing timing information, including "Timing Constraints were met.", "Jitter: 1.985 ns", and "Frequency: 502.765 MHz".
- Implemented Partitions:** A panel showing the partitioning of resources, with "team1\_inst" listed.
- Command Line:** A panel at the bottom showing the command line for the implementation process, including the path to the PlanAhead executable and the project files.

# RTL Project



# RTL Project

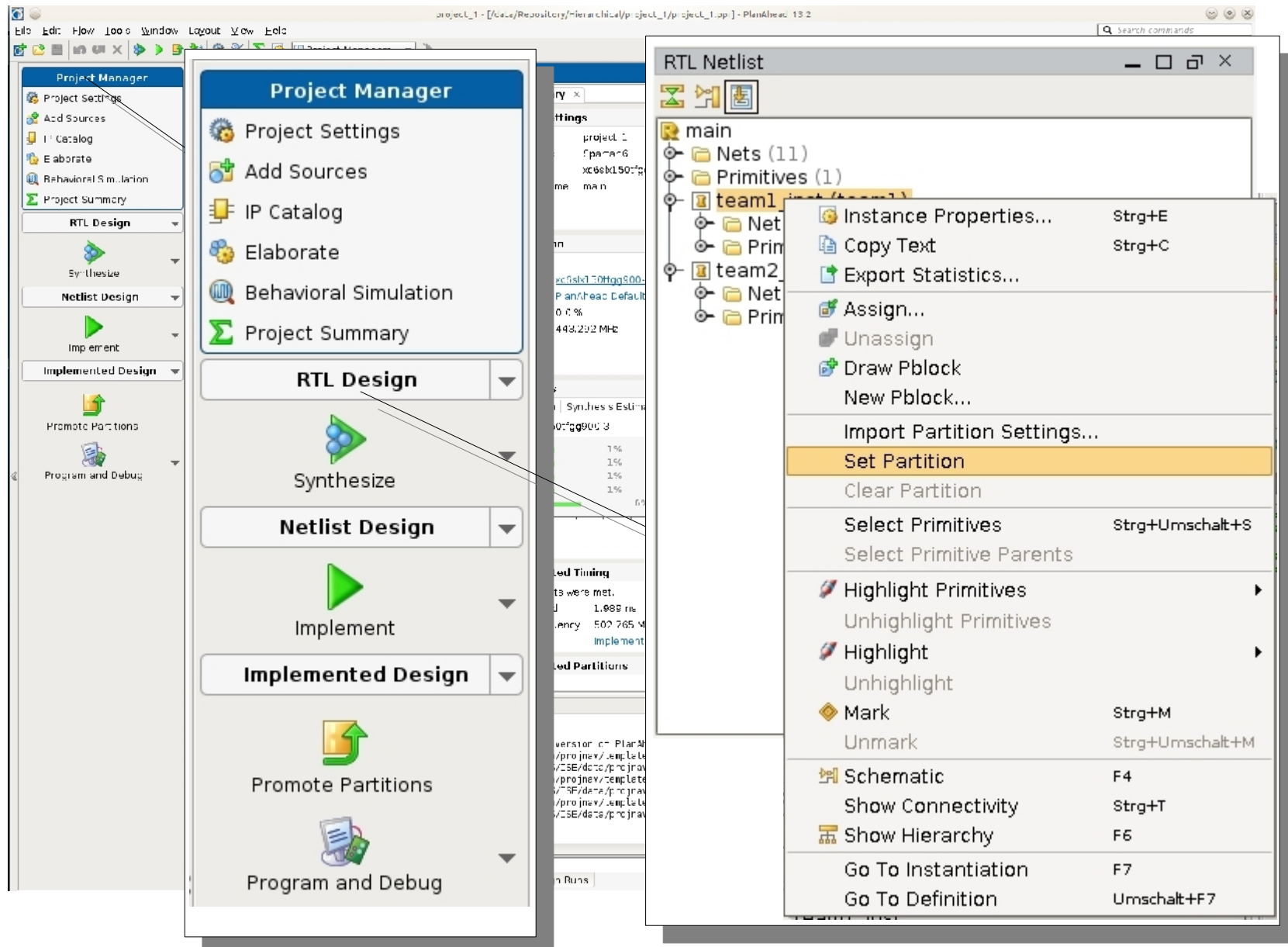
The image shows a screenshot of a design tool interface. On the left, the **Project Manager** window is open, displaying a list of project actions: Project Settings, Add Sources, IP Catalog, Elaborate, Behavioral Simulation, and Project Summary. Below this list are four main design stages: **RTL Design** (with a Synthesize button), **Netlist Design** (with an Implement button), **Implemented Design** (with Promote Partitions and Program and Debug buttons), and **RTL Design** (with a Synthesize button). A red arrow points from the **RTL Design** dropdown menu to the **RTL Netlist** window on the right.

The **RTL Netlist** window shows a hierarchical tree structure of the design. The root is **main**, which contains:

- Nets (11)
- Primitives (1)
- team1\_inst (team1) (highlighted in yellow)
- Nets (67)
- Primitives (4)
- team2\_inst (team2)
- Nets (35)
- Primitives (3)

At the bottom of the RTL Netlist window, there are tabs for **Sources**, **RTL Netlist** (selected), and **Timing Constr..**

# RTL Project

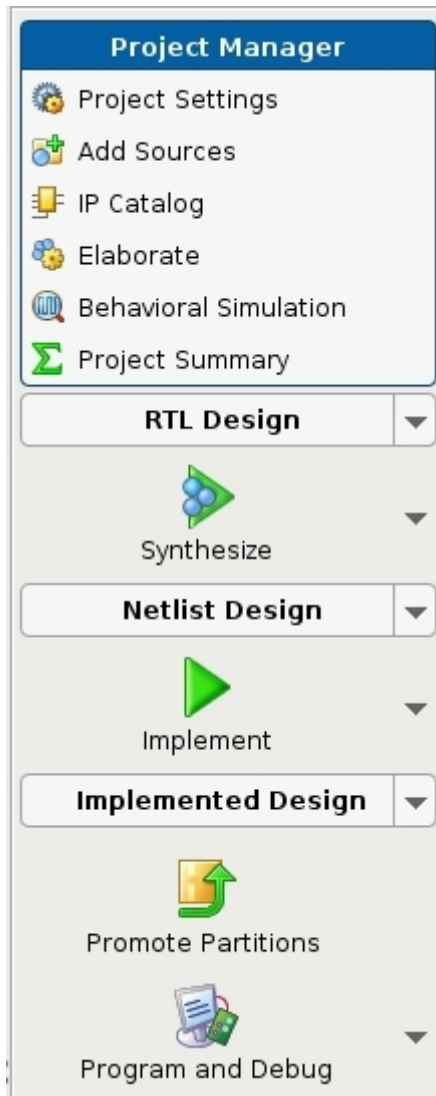


# RTL Project

The image displays a screenshot of an FPGA design tool interface. The top window, titled "RTL Netlist", shows a hierarchical tree structure of the design. The "main" folder contains "Nets (11)", "Primitives (1)", and "clkbufds (IBUFGDS)". Under "Primitives", there are two instances: "team1\_inst" and "team2\_inst". A context menu is open over "team1\_inst", listing various actions such as "Instance Properties...", "Copy Text", "Export Statistics...", "Assign...", "Unassign", "Draw Pblock", "New Pblock...", "Import Partition Settings...", "Set Partition", "Clear Partition", "Select Primitives", "Select Primitive Parents", "Highlight Primitives", "Unhighlight Primitives", "Highlight", "Unhighlight", "Mark", "Unmark", "Schematic", "Show Connectivity", "Show Hierarchy", "Go To Instantiation", and "Go To Definition". The bottom window, titled "RTL Schematic", shows a detailed view of the RTL schematic. It features a grid of logic resources with various components and connections. Two specific blocks are highlighted in purple: "pblock team1\_inst" and "pblock team2\_inst". The schematic also shows various logic elements, registers, and interconnects.



# RTL Project



# RTL Project

The screenshot displays the Xilinx ISE Project Manager interface for an RTL Design project. The left sidebar shows the Project Manager with sections for RTL Design, Netlist Design, and Implemented Design. The main window is titled "RTL Design - rtl\_1 - xc6slx150tfgg900-3 (active)".

**RTL Design**

- IP Catalog
- Elaborate
- Resource Estimation
- Power Estimation
- Run DRC
- Run Noise Analysis
- Behavioral Simulation

**Netlist Design**

- Implement

**Implemented Design**

- Promote Partitions
- Program and Debug

**Promoted Partitions**

Promoted Directory	Run	Promoted on	Description
...ote/Ximpl_1 (2)	impl_1	7/18/11 2:52 PM	
team1_inst			
team2_inst			
...te/Xsynth_1 (2)	synth_1	7/18/11 2:52 PM	
team1_inst			
team2_inst			

**Implementation Settings...**

- Create New Implementation Runs...
- Specify Partitions...

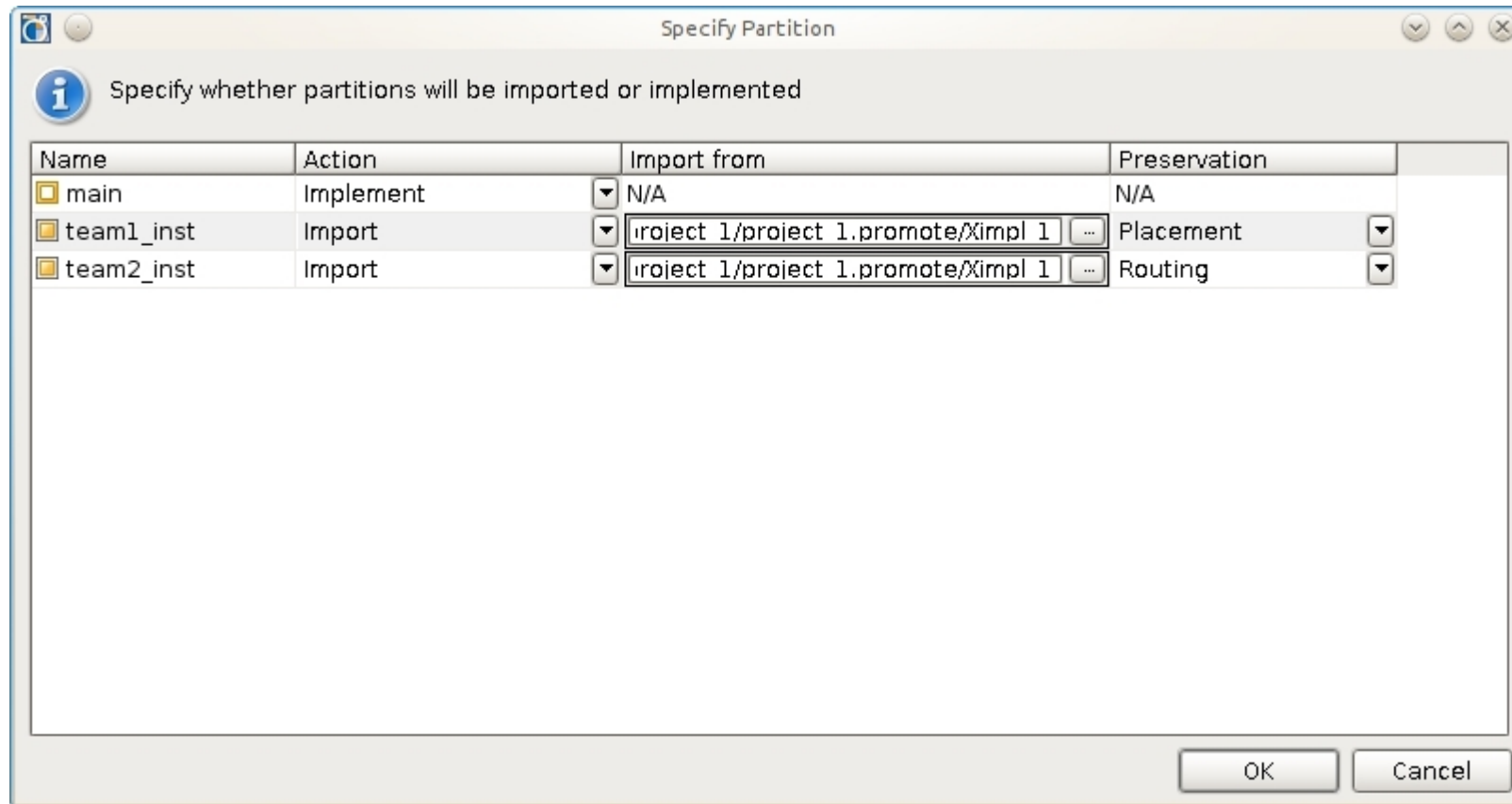
**Instance Properties**

team2\_inst

Full Name: team2\_inst  
Pblock: pblock\_team2\_inst  
Cell: team2  
Type: Others

General | Statistics | Pins | Children | Attributes

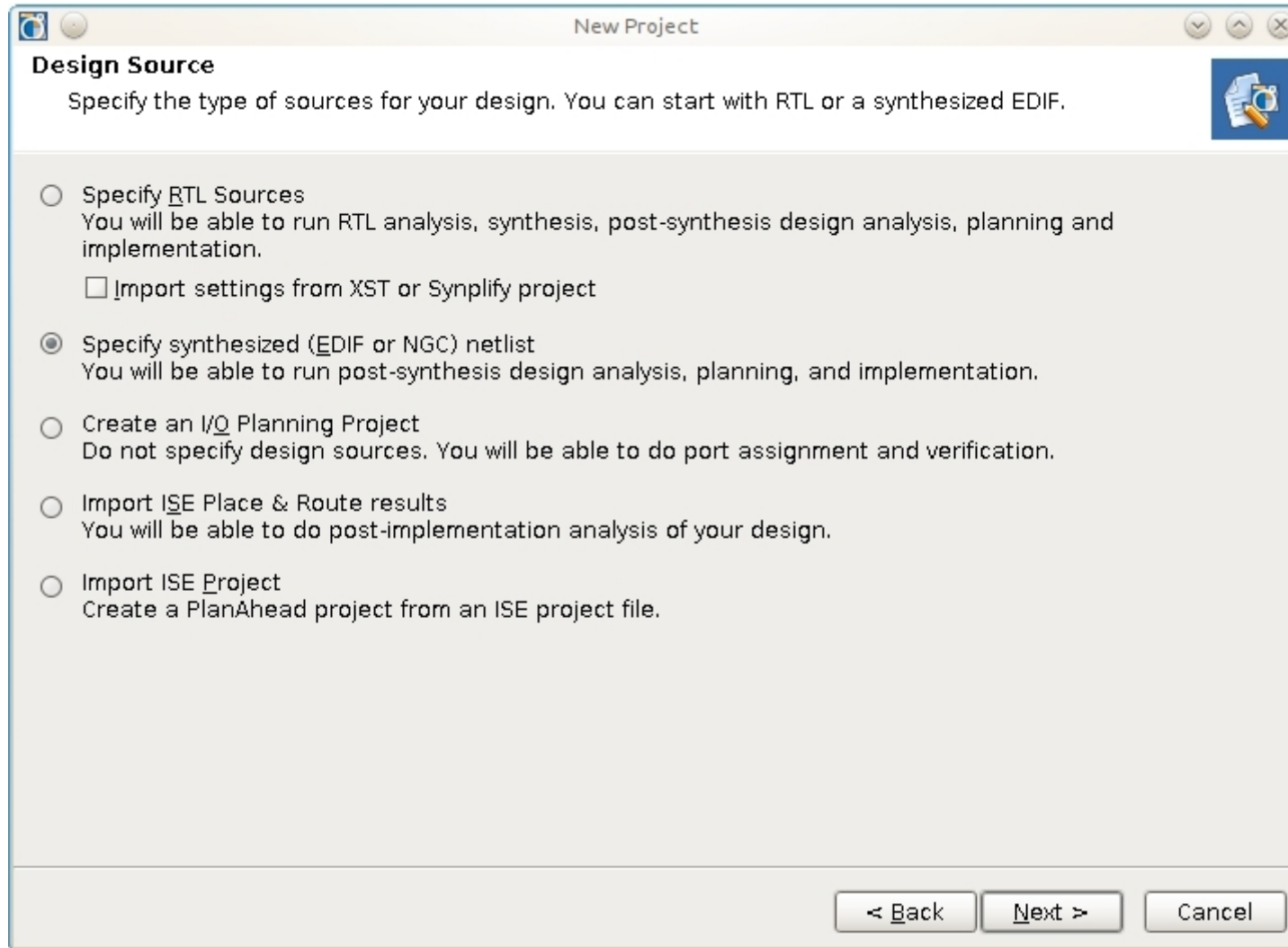
# RTL Project



### 3 Levels of Design Preservation:

- Synthesis
- Placement
- Routing

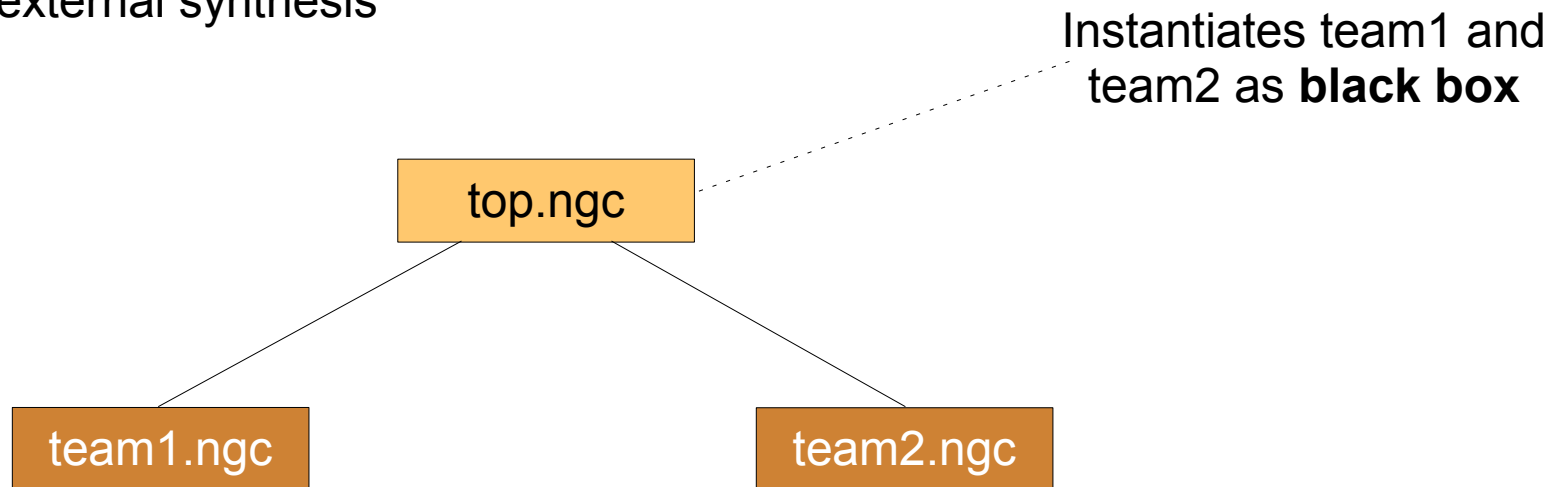
# NGC Project



# NGC Project

## *Differences to the RTL Project:*

**Sources:** NGC files (netlists)  
==> Requires external synthesis

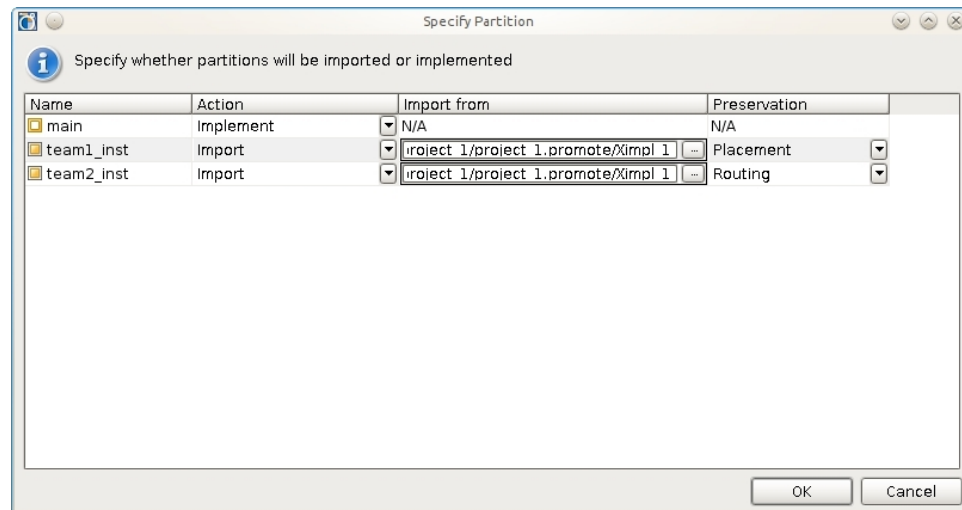
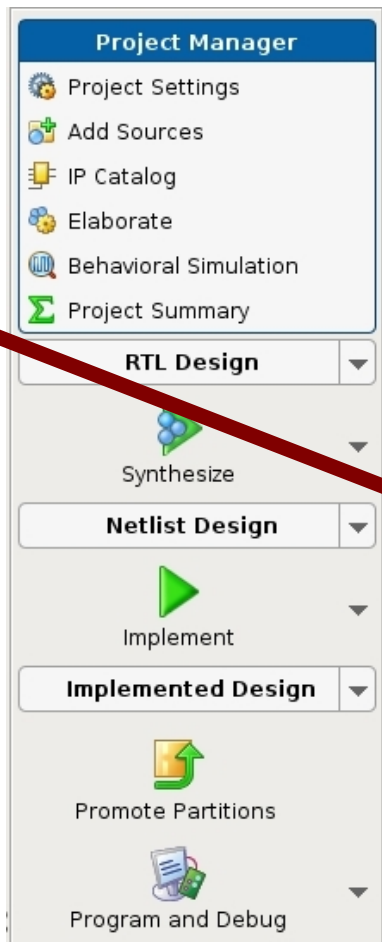


general Synthesis hints:

- deactivate automatically generated I/O buffers
- instantiate all I/O buffers directly

# NGC Project

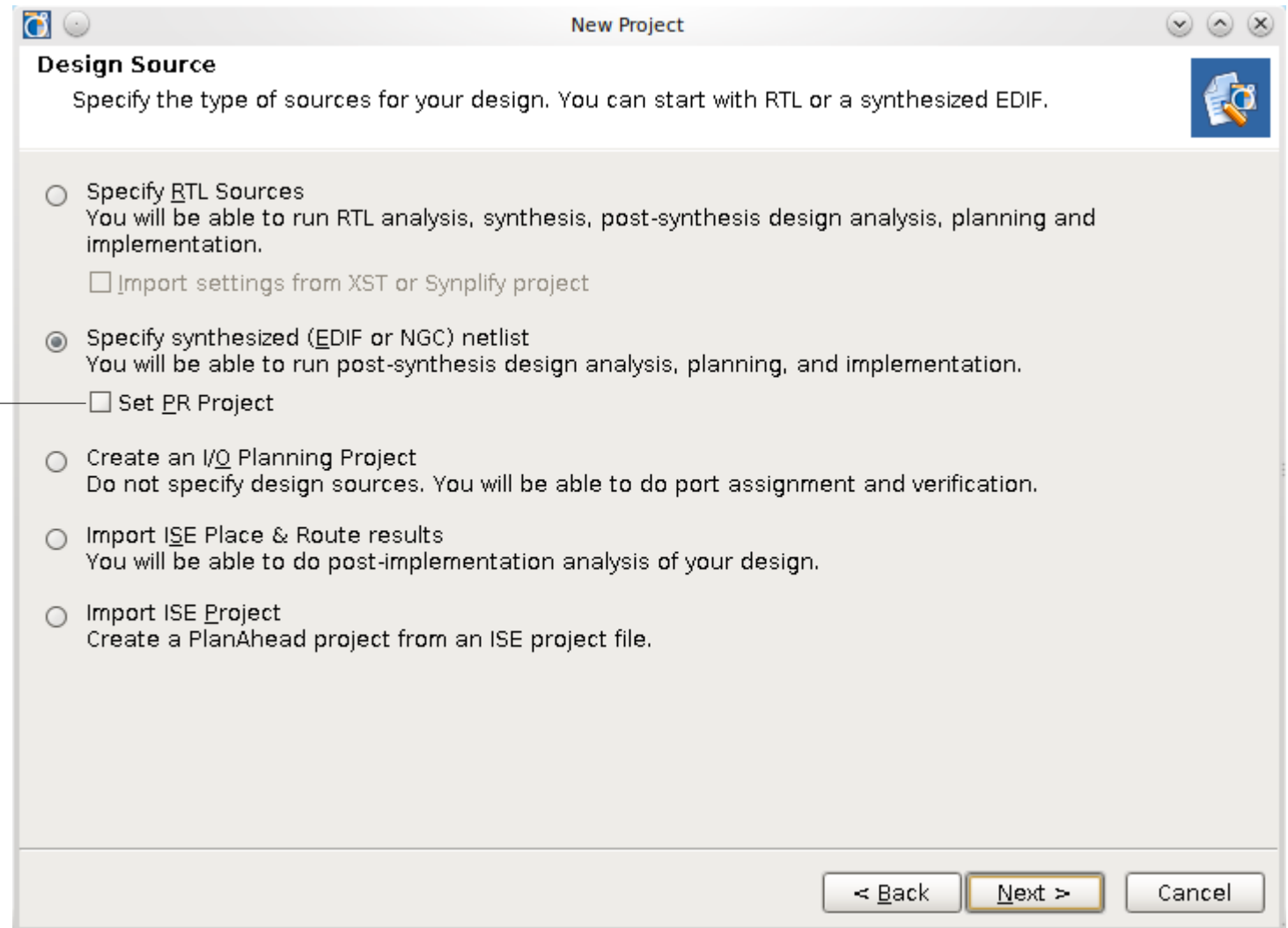
## *Differences to the RTL Project:*



### 3 Levels of Design Preservation:

- Synthesis (same as Implement)
- Placement
- Routing

# Partial Reconfiguration



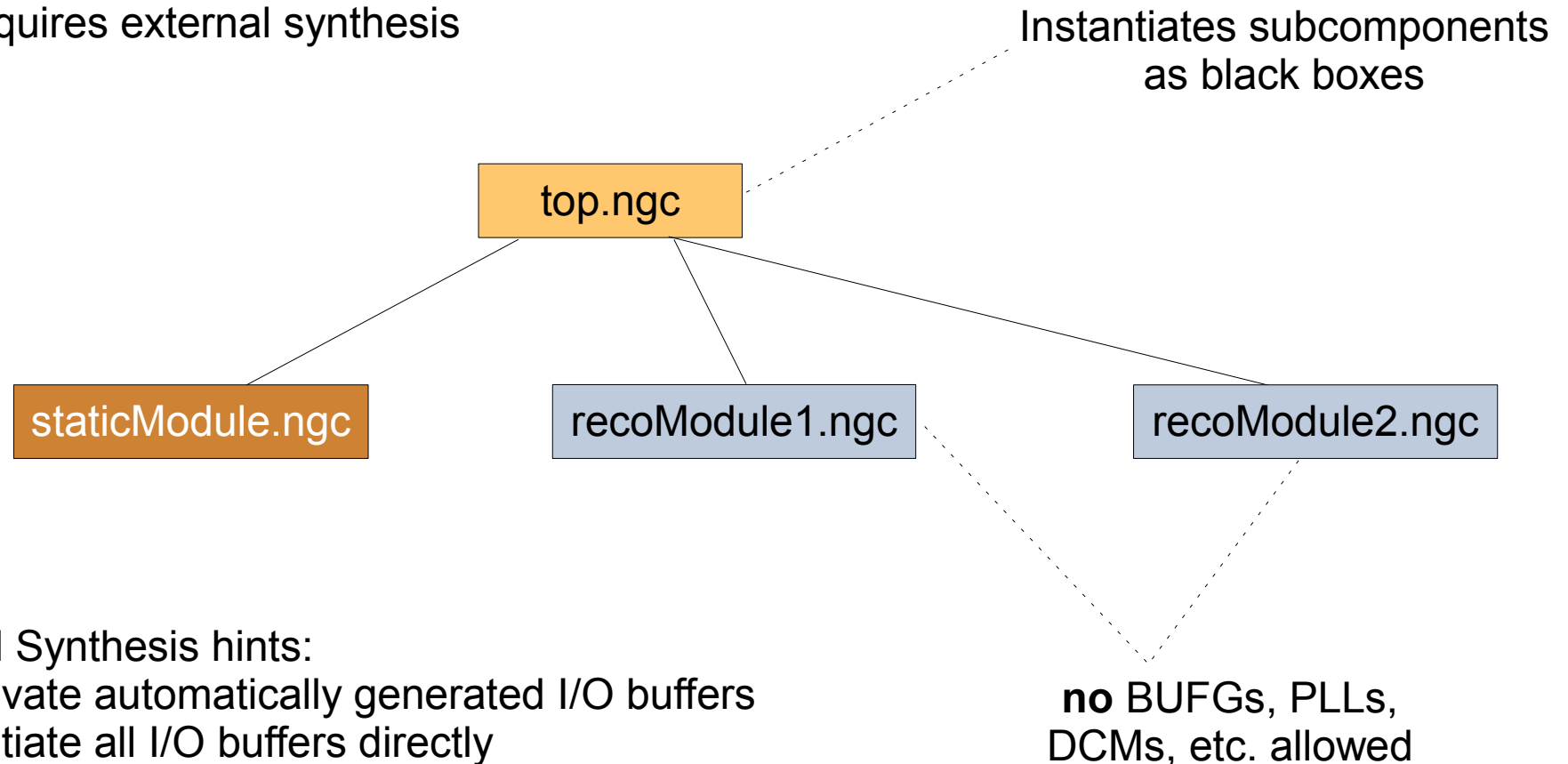
Requires a special  
PR-License

No patches needed  
any longer!

# Partial Reconfiguration

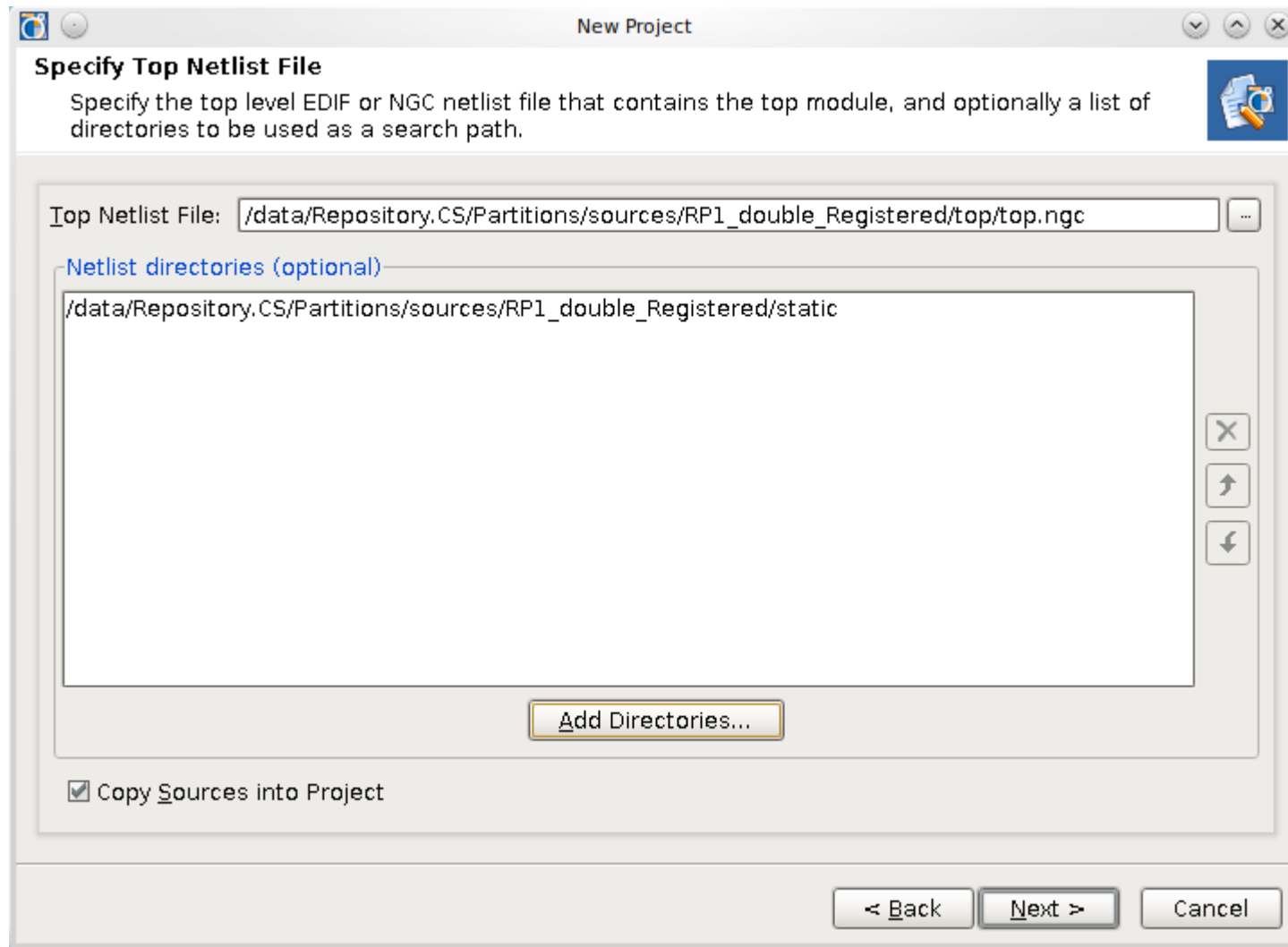
## *PR designs are NGC designs*

**Sources:** NGC files (netlists)  
==> Requires external synthesis





# Partial Reconfiguration



# Partial Reconfiguration

The screenshot displays the PlanAhead 13.2 software interface for a project named 'testProject'. The main window is titled 'testProject - [/data/Repository/CS/testProject/testProject.ppr] - PlanAhead 13.2'. The interface is divided into several panes:

- Project Manager (Left):** Contains 'Project Settings', 'Add Sources', and 'Project Summary' buttons. Below these are 'Netlist Design', 'Implement' (with a green play button), 'Implemented Design', 'Promote Partitions', and 'Program and Debug' options.
- Sources (Top Middle):** Shows a tree view of 'Design Sources (2)' including 'NGC (2)' (with sub-items 'top.ngc (top)' and 'staticModule.ngc'), 'Constraints (1)' (with sub-item 'constrs\_1'), and 'top.ucf (target)'.
- Source File Properties (Bottom Middle):** Displays details for 'top.ucf':
  - Location: /data/Repository/CS/testProject/t
  - Type: UCF
  - Size: 0.3 kb
  - Modified: 7/14/11 3:51:31 PM
  - Copied To: testProject.srcs/constrs\_1/imports
- Project Summary (Right):** Provides an overview of the project's status and configuration:
  - Project Settings:** Project Name: testProject, Product Family: Virtex4, Default Part: xc4vx20ff672-11.
  - Project State:** Status: Ready, Messages: 0 errors, 0 critical warnings, 0 warnings. Next Step: [Implement](#).
  - Compilation:** Implementation Part: [xc4vx20ff672-11](#), Strategy: [ISE Defaults](#).
  - Resources:** Resource information is not available.
  - Implemented Timing:** Timing information is not available. Next: [Implement](#).
  - Implemented Partitions:** Partition information is not available. Next: [Specify Partitions](#), [Implement](#).
- Tcl Console (Bottom):** Shows the following commands:

```
create_project testProject /data/Repository/CS/testProject -part xc4vx20ff672-11
set_property design_mode GateLvl [current_fileset]
set_property edif_top_file /data/Repository/CS/Partitions/sources/RP1_double_Registered/top/top.ngc [current_fileset]
import_files -force -norecurse /data/Repository/CS/Partitions/sources/RP1_double_Registered/static /data/Repository/CS/Partitions/sources/RP1_double_Registered/static
import_files -fileset constrs_1 -force -norecurse /data/Repository/CS/Partitions/sources/RP1_double_Registered/top/top.ucf
set_property target_constrs_file /data/Repository/CS/testProject/testProject.srcs/constrs_1/imports/top/top.ucf [current_fileset]
set_property name config_1 [current_run]
set_property is_partial_reconfig true [current_project]
remove_files /data/Repository/CS/testProject/testProject.srcs/sources_1/imports/RP1_double_Registered/static/static.ngc
```

The bottom right corner of the window shows 'Partial Reconfiguration Flow'.

# Partial Reconfiguration

The screenshot displays the PlanAhead 13.2 software interface for a project named 'testProject'. The main window shows the 'Project Manager' on the left, the 'Project Summary' on the right, and a 'Sources' window in the foreground. The 'Project Summary' indicates the project is 'Ready' with no errors or warnings. The 'Sources' window shows a tree structure with 'Design Sources (2)' containing 'NGC (2)' (top.ngc and staticModule.ngc) and 'Constraints (1)' (constrs\_1). The 'Project Summary' also shows 'Implementation' details: Part: xc4vfx20ff672-11, Strategy: ISE Defaults. The 'Console' window at the bottom shows the command: `partial_reconfig true [current_project]`. The status bar at the bottom right indicates 'Partial Reconfiguration Flow'.

# Partial Reconfiguration

The screenshot displays the Xilinx ISE software interface. The main window is titled "Netlist Design - netlist\_1 - xc4vfx20ffo/2-11 (active)". The left sidebar contains the "Project Manager" with options like "Resource Estimation", "Power Estimation", "Run DRC", "Report: Timing", "Stack Histogram", and "Set up ChipScope". The "Implement" button is visible. The central area shows a "Netlist" window with a tree view containing "top", "Nets (27)", "Primitives (10)", "reccModule1 (recoModule)", "reccModule2 (recoModule)", and "stat cModule1 (staticModule)". Below the netlist is a "Properties" window. The right side of the interface shows a "Device" window displaying a grid-based device configuration. The bottom of the window features a "Tcl Console" with the following output:

```
INFO: [ArchReader-6] Loading clock buffers from /data/Xilinx_NFS/13.2/ISE_DS/PlanAhead/parts/xilinx/virtex4/virtex4fx/xc4vfx20/ClockBuffer...  
INFO: [ArchReader-3] Loading package from /data/Xilinx_NFS/13.2/ISE_DS/PlanAhead/parts/xilinx/virtex4/virtex4fx/xc4vfx20/ff672/Package.xml  
INFO: [ArchReader-4] Loading io standards from /data/Xilinx_NFS/13.2/ISE_DS/PlanAhead/parts/xilinx/virtex4/virtex4fx/xc4vfx20/ff672/IOStandards.xml  
INFO: [ArchReader-5] Loading pkg sso from /data/Xilinx_NFS/13.2/ISE_DS/PlanAhead/parts/xilinx/virtex4/virtex4fx/xc4vfx20/ff672/SSORules.xr  
INFO: [GDRG-0] Loading list of drcs for the architecture : /data/Xilinx_NFS/13.2/ISE_DS/PlanAhead/parts/xilinx/virtex4/drc.xml  
INFO: [LID-0] Reading timing library /data/Xilinx_NFS/13.2/ISE_DS/PlanAhead/parts/xilinx/virtex4/virtex4fx/virtex4fx-11.lib  
INFO: [LIB-1] Done reading timing library /data/Xilinx_NFS/13.2/ISE_DS/PlanAhead/parts/xilinx/virtex4/virtex4fx/virtex4fx-11.lib  
Parsing UCF File [/data/Repository/CS/tesProject/tesProject/srcs/consts_1/imports/top/top.ucf]  
Finished Parsing UCF File [/data/Repository/CS/tesProject/tesProject/srcs/consts_1/imports/top/top.ucf]  
open_netlist_design: Time (s): 4.960w 0.190s 8.060w. Memory (MB): 1048.160w 0.000g
```

The bottom right corner of the interface has a button labeled "Partial Reconfiguration Flow".

# Partial Reconfiguration

The screenshot displays the Xilinx ISE software interface for a project named 'testProject'. The main window shows a 'Netlist Design' for 'netlist\_1'. The design hierarchy includes 'top', 'Nets (27)', 'Primitives (10)', 'recoModule1 (recoModule)', 'recoModule2 (recoModule)', and 'staticModule1 (staticModule)'. A 'Project Manager' sidebar on the left lists various analysis tools like Resource Estimation, Power Estimation, Run DRC, Report: Timing, Stack Histogram, and Set up ChipScope. A 'Project Summary' and 'Device' window on the right shows a physical implementation of the design on a device, with a grid of colored lines representing the routing. A 'Timing Co.' window is also visible. At the bottom, a console window displays the following text:

```
clock buffers from /data/Xilinx_NFS/13.2/ISE_DS/PlanAhead/parts/xilinx/virtex4/virtex4/xc4vfx20/ClockBuffer
package from /data/Xilinx_NFS/13.2/ISE_DS/PlanAhead/parts/xilinx/virtex4/virtex4/xc4vfx20/ff672/Package.xml
io standards from /data/Xilinx_NFS/13.2/ISE_DS/PlanAhead/parts/xilinx/virtex4/virtex4/xc4vfx20/ff672/IOStandards.xml
pkg sso from /data/Xilinx_NFS/13.2/ISE_DS/PlanAhead/parts/xilinx/virtex4/virtex4/xc4vfx20/ff672/SSORules.xr
of drcs for the architecture : /data/Xilinx_NFS/13.2/ISE_DS/PlanAhead/parts/xilinx/virtex4/drc.xml
library /data/Xilinx_NFS/13.2/ISE_DS/PlanAhead/parts/xilinx/virtex4/virtex4/xc4vfx20/ff672/lib
timing library /data/Xilinx_NFS/13.2/ISE_DS/PlanAhead/parts/xilinx/virtex4/virtex4/xc4vfx20/ff672/lib
library /data/Xilinx_NFS/13.2/ISE_DS/PlanAhead/parts/xilinx/virtex4/virtex4/xc4vfx20/ff672/lib
library /data/Repository/CS/testProject/testProject/srcs/consts_1/imports/top/top.ucf]
data/Repository/CS/testProject/testProject/srcs/consts_1/imports/top/top.ucf]
): 4.960u 0.190s 8.060w. Memory (MB): 1048.160p 0.000g
```

# Partial Reconfiguration

The screenshot displays the Xilinx ISE software interface. The main window is titled "Netlist Design - netlist\_1 - xc4vfx20ff672-11 (active)". A context menu is open over a reconfigurable module in the netlist tree, listing various actions such as "Instance Properties...", "Copy Text", "Export Statistics...", "Set Partition...", "Highlight Primitives", and "Mark". The "Set Partition..." option is highlighted. The background shows a device configuration grid with a central black area representing the reconfigurable module. The Tcl Console window at the bottom shows logs for loading standards, packages, and timing libraries, and parsing UCF files.

File Edit Flow Tools Window Layout View Help

Search commands

Ready

Project Manager

Netlist Design

Resource Estimation

Power Estimation

Run DRC

Report Timing

Slack Histogram

Set up ChipScope

Implement

Implemented Design

Promote Partitions

Program and Debug

Netlist

top

Nets (27)

Primitives (10)

recoModule (reconfigurableModule)

recoModule

static

Instance Properties... Ctrl+E

Copy Text Ctrl+C

Export Statistics...

Unplace Ctrl+U

Swap locations Ctrl+H

Assign...

Unassign

Draw Pblock

New Pblock...

Set Partition...

Clear Partition

Unset Reconfigurable Partition

Add Reconfigurable Module...

Select Primitives Ctrl+Shift+S

Select Primitive Parents

Highlight Primitives

Unhighlight Primitives

Highlight

Unhighlight

Mark Ctrl+M

Unmark Ctrl+Shift+M

Fix Instances

Unfix Instances

General

Cross-probe to FPGA Editor

Schematic F4

Show Connectivity Ctrl+T

Show Hierarchy F6

Tcl Console

INFO: [ArchReader-4] Loading io standards from /data/Xilinx\_NFS/13.2/ISE\_DS/PlanAhead/parts/xilinx/virtex4/virtex4fx/xc4vfx20/ClockBuffer...  
INFO: [ArchReader-5] Loading pkg sso from /data/Xilinx\_NFS/13.2/ISE\_DS/PlanAhead/parts/xilinx/virtex4/virtex4fx/xc4vfx20/ff672/Package.xml  
INFO: [GDRC-0] Loading list of drcs for the architecture : /data/Xilinx\_NFS/13.2/ISE\_DS/PlanAhead/.parts/xilinx/virtex4/drc.xml  
INFO: [LIB-0] Reading timing library /data/Xilinx\_NFS/13.2/ISE\_DS/PlanAhead/parts/xilinx/virtex4/virtex4fx/virtex4fx-11.lib .  
INFO: [LIB-1] Done reading timing library /data/Xilinx\_NFS/13.2/ISE\_DS/PlanAhead/parts/xilinx/virtex4/virtex4fx/virtex4fx-11.lib .  
Parsing UCF File [/data/Repository.CS/testProject/testProject.srscs/constrs\_1/imports/top/top.ucf]  
Finished Parsing UCF File [/data/Repository.CS/testProject/testProject.srscs/constrs\_1/imports/top/top.ucf]  
open\_netlist\_design: Time (s): 4.960u 0.190s 8.060w. Memory (MB): 1048.160p 0.000g

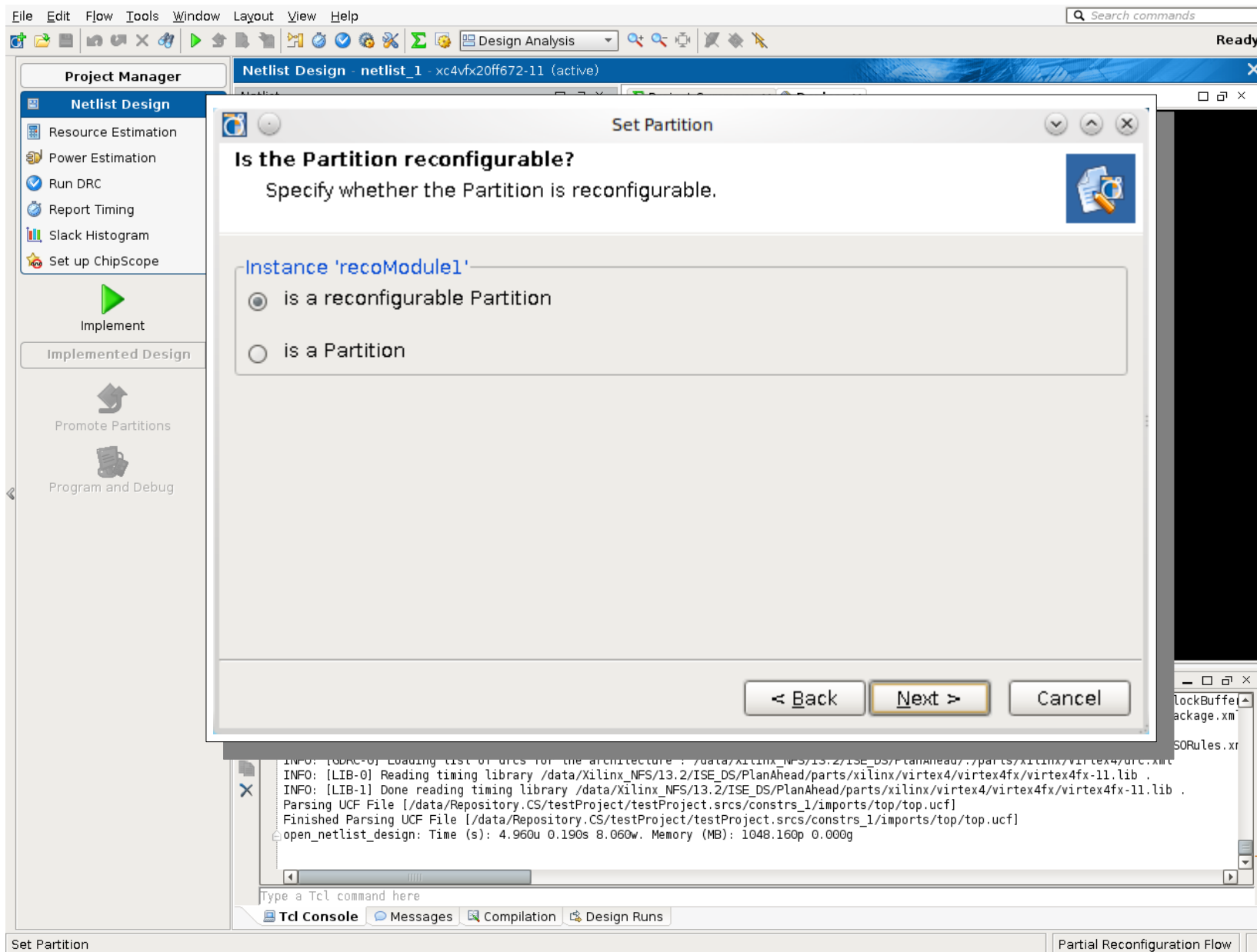
Type a Tcl command here

Tcl Console Messages Compilation Design Runs

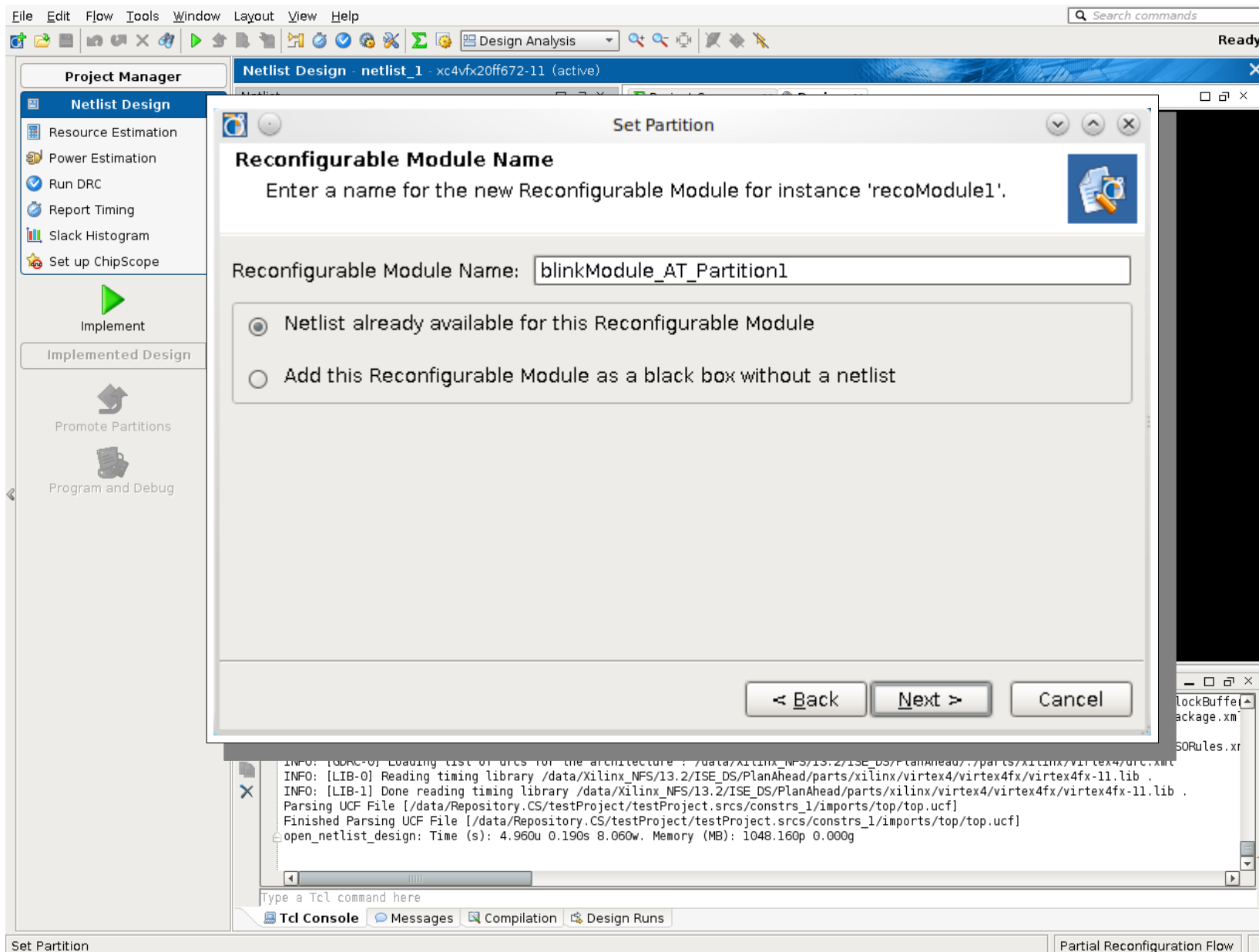
Set Partition

Partial Reconfiguration Flow

# Partial Reconfiguration

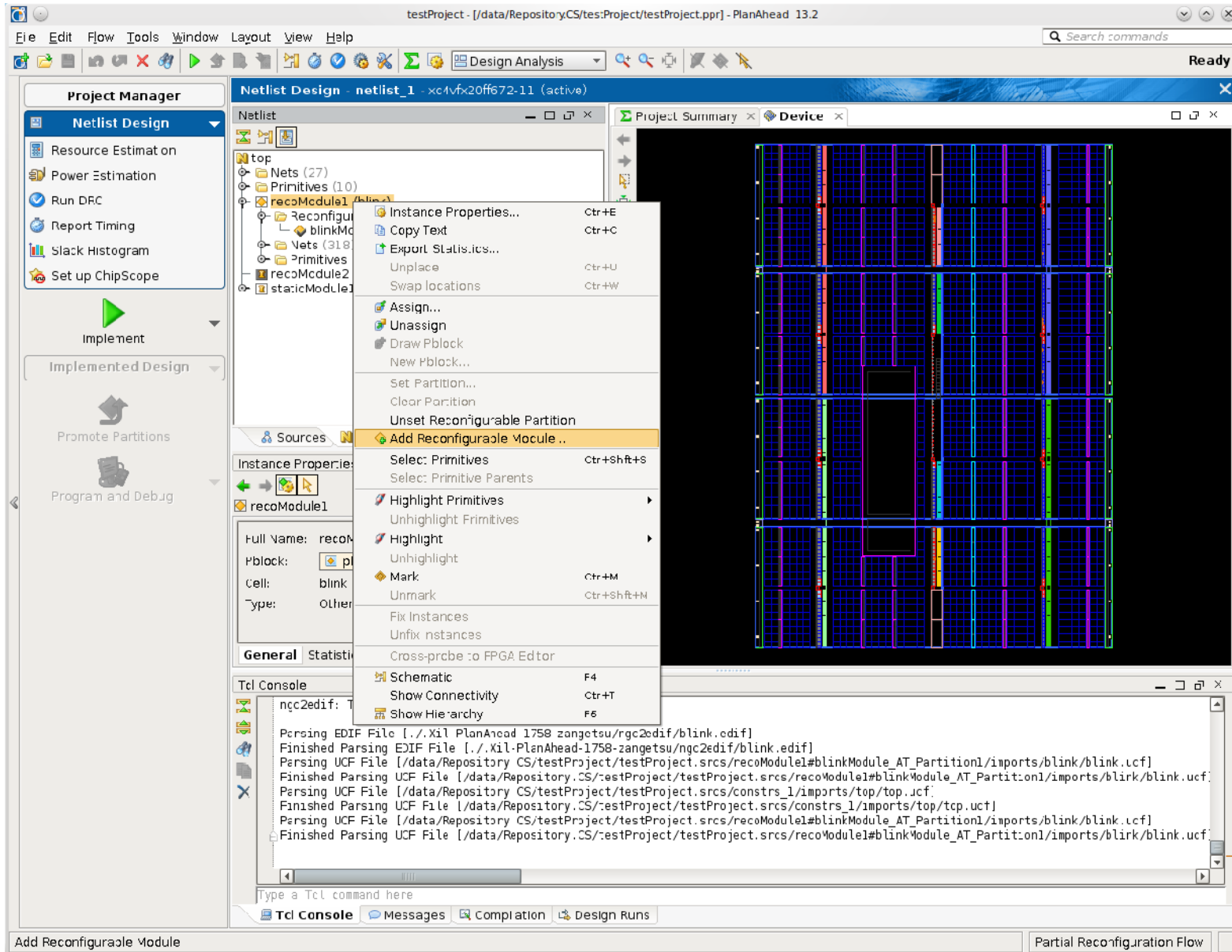


# Partial Reconfiguration





# Partial Reconfiguration



# Partial Reconfiguration

The screenshot displays the Xilinx PlanAhead 13.2 software interface. The main window is titled "testProject - [/data/Repository/CS/testProject/testProject.ppr] - PlanAhead 13.2". The interface is divided into several panes:

- Project Manager:** Shows the "Netlist Design" tab with options like "Resource Estimation", "Power Estimation", "Run DRC", "Report Timing", "Slack Histogram", and "Set Up ChipScope". A green play button labeled "Implement" is visible.
- Netlist Design - netlist\_1 - xc4vx20f672-1: (active):** Displays a hierarchical netlist structure. The "recoModule1" is highlighted, showing its internal components: "Reconfigurable Modules (2)", "Nets (318)", and "Primitives (317)".
- Instance Properties:** Shows details for "recoModule1", including "Full Name: recoModule1", "Pblock: pblock\_recoModule1", "Cell: blink", and "Type: Others".
- Device View:** A graphical representation of the device architecture. A tooltip "Set Pblock Size" is overlaid, stating "Press & drag on Device View to set Pblock size".
- Tcl Console:** Displays the following commands and output:

```
Finished Parsing UCF File [/data/Repository/CS/testProject/testProject.srcs/constrs_1/imports/top/top.ucf]
Parsing UCF File [/data/Repository/CS/testProject/testProject.srcs/recoModule1#blinkModule_AT_Partition1/imports/blink/blink.ucf]
Finished Parsing UCF File [/data/Repository/CS/testProject/testProject.srcs/recoModule1#blinkModule_AT_Partition1/imports/blink/blink.ucf]
Parsing UCF File [/data/Repository/CS/testProject/testProject.srcs/recoModule2#blinkModule_AT_Partition2/imports/blink/blink.ucf]
Finished Parsing UCF File [/data/Repository/CS/testProject/testProject.srcs/recoModule2#blinkModule_AT_Partition2/imports/blink/blink.ucf]
load_reconfig_modules: Time (s): 3.7600 0.120s 5.530w. Memory (MB): 1048.16cp 0.000g
create_reconfig_nocule -name dimModule_AT_Partition2 -cell recoModule2
create_reconfig_nocule: Time (s) 3.5800 0.080s 5.010w. Memory (MB): 1050.168p 0.000g
set_property ed_i_top_file /data/Repository/CS/Partitions/sources/RP1_double_Registered/dim/din.ngc [get_filesets recoModule2#dimModule_AT_Partition2]
import_files -filesel recoModule2#dimModule_AT_Partition2 -force -norecuse [/data/Repository/CS/Partitions/sources/RP1_double_Registered/
```

At the bottom of the window, there is a status bar with the text "Press & drag on Device View to set Pblock size" and a button labeled "Partial Reconfiguration Flow".

# Partial Reconfiguration

The screenshot displays the Xilinx ISE software interface for a project named "testProject". The main window is titled "Netlist Design - netlist\_1 - xc4vx20f672-1: (active)". The interface is divided into several panes:

- Project Manager:** Shows the project structure with "Netlist Design" selected.
- Netlist Design:** Displays a hierarchical tree of components. The "recoModule1 (blink)" component is highlighted. The tree structure is as follows:
  - top
    - Nets (27)
    - Primitives (10)
    - recoModule1 (blink)
      - Reconfigurable Modules (2)
        - blinkModule\_AT\_Partition1
        - dimModule\_AT\_Partition1
      - Nets (318)
      - Primitives (317)
    - recoModule2 (blink)
      - Reconfigurable Modules (2)
        - blinkModule\_AT\_Partition2
        - dimModule\_AT\_Partition2
      - Nets (318)
      - Primitives (317)
    - staticModule1 (staticModule)

- Project Summary:** Shows resource usage statistics for the design.
- recoModule1 (blink)
  - blinkModule\_AT\_Partition1: 3.760u 0.120s 5.530w. Memory (MB): 1048.168p 0.000g
  - dimModule\_AT\_Partition1: 3.580u 0.080s 5.010w. Memory (MB): 1050.168p 0.000g
- recoModule2 (blink)
  - blinkModule\_AT\_Partition2: 3.760u 0.120s 5.530w. Memory (MB): 1048.168p 0.000g
  - dimModule\_AT\_Partition2: 3.580u 0.080s 5.010w. Memory (MB): 1050.168p 0.000g
- Device View:** Shows a grid of logic blocks with a highlighted area for reconfiguration. A tooltip "Set Pblock Size" is visible, indicating that the user can press and drag on the Device View to set the pblock size.

# Partial Reconfiguration

The screenshot displays the PlanAhead 13.2 software interface for a project named 'testProject'. The main window is titled 'Netlist Design - netlist\_1 - xc4vx20f672-1: (active)'. The interface is divided into several panes:

- Project Manager:** Located on the left, it shows a tree view under 'Netlist Design' with options like 'Resource Estimation', 'Power Estimation', 'Run DRC', 'Report Timing', 'Slack Histogram', and 'Set Up ChipScope'. Below these are buttons for 'Implement', 'Promote Partitions', and 'Program and Debug'.
- Netlist Design:** The central pane shows a hierarchical netlist structure. The root is 'top', which contains 'Nets (27)', 'Primitives (10)', and two 'recoModule' instances. 'recoModule1' contains 'Reconfigurable Modules (2)' (blinkingModule\_AT\_Partition1 and dimModule\_AT\_Partition1), 'Nets (318)', and 'Primitives (317)'. 'recoModule2' has a similar structure with Partition2.
- Instance Properties:** Below the netlist, it shows properties for 'recoModule1', including 'Full Name: recoModule1', 'Pblock: pblock\_recoModule1', 'Cell: blink', and 'Type: Others'.
- Tcl Console:** At the bottom, it shows the execution of various Tcl commands, including parsing UCF files and creating/reconfiguring modules. The console output includes:

```
Finished Parsing UCF File [/data/Repository.CS/testProject/testProject.srcs/cons_rsr_1/imports/top/top.ucf]
Parsing UCF File [/data/Repository.CS/testProject/testProject.srcs/recoModule1#blinkModule_AT_Partition1/imports/blink/blink.ucf]
Finished Parsing UCF File [/data/Repository.CS/testProject/testProject.srcs/recoModule1#blinkModule_AT_Partition1/imports/blink/blink.ucf]
Parsing UCF File [/data/Repository.CS/testProject/testProject.srcs/recoModule2#blinkModule_AT_Partition2/imports/blink/blink.ucf]
Finished Parsing UCF File [/data/Repository.CS/testProject/testProject.srcs/recoModule2#blinkModule_AT_Partition2/imports/blink/blink.ucf]
load_reconfig_modules: Time (s): 3.760u 0.120s 5.530w. Memory (MB): 1048.16cp 0.000g
create_reconfig_nocule -name dimModule_AT_Partition2 -cell recoModule2
create_reconfig_nocule: Time (s) 3.580u 0.080s 5.010w. Memory (MB): 1050.168p 0.000g
set_property edi_top_file /data/Repository.CS/Partitions/sources/RP1_double_Registered/dim/dim.ngc [get_filesets recoModule2#dimModule_AT_Partition2]
import_files -filesel recoModule2#dimModule_AT_Partition2 -force -norecuse {/data/Repository.CS/Partitions/sources/RP1_double_Registered/}
```

Two callout boxes with the text 'Set Pblock Size Press & drag on Device View to set Pblock size' are overlaid on the right side of the interface, pointing to the 'Device View' area. The 'Device View' itself shows a grid of colored blocks representing the hardware resources.

# Partial Reconfiguration

The screenshot displays the Xilinx PlanAhead 13.2 software interface. The main window is titled "testProject - [data/Repository/CS/testProject/testProject.ppr] - PlanAhead 13.2". The interface is divided into several panes:

- Project Manager:** Contains a "Netlist Design" section with options like "Resource Estimation", "Power Estimation", "Run DRC", "Report Timing", "Slack Histogram", and "Set up ChpScope". Below these are "Implement", "Promote Partitions", and "Program and Debug" buttons.
- Netlist Design:** Shows a hierarchical tree view of the netlist. The root is "top", which contains "Nets (27)", "Primitives (1 C)", "recoModule1 (blirk)", "Reconfigurable Modules (2)", "recoModule2 (blirk)", "Reconfigurable Modules (2)", and "staticModule1 (staticModule)".
- Tile Properties:** Displays properties for the selected tile "CLB\_X34Y26", including Name, Type (CLB), Row (47), Column (73), and Number of sites (4).
- Device Configuration:** A large grid representing the device layout. The grid is color-coded to show different components: "recoModule1", "recoModule2", "staticModule1", and "pblock\_recoModule1".
- Tcl Console:** Shows a series of Tcl commands used for configuration, such as "import\_files", "resize\_pblock", "create\_pblock", and "resize\_pblock".

The status bar at the bottom indicates "Tile: CLB\_X34Y26" and "Partial Reconfiguration Flow".

# Partial Reconfiguration

The screenshot displays the Xilinx ISE 13.2 software interface for a project named "PR\_BlinkDim\_with\_static". The main window shows the "Netlist Design" for "netlist\_1" with two configurations: "config\_1" and "config\_2".

**Configurations Table:**

Configuration	Module Variant	Status
config_1 (4)		Implementation Out-of-date
Static Logic		Implement
recoModule2	blinkModule_Partition2	Implement
recoModule1	blinkModule_Partition1	Implement
staticModule1		Implement
config_2 (4)		Implementation Out-of-date
Static Logic		Import
recoModule2	dimModule_Partition2	Implement
recoModule1	dimModule_Partition1	Implement
staticModule1		Import

The "Configuration Module State Properties" window shows the selected configuration "config\_2" and instance "staticModule1" with an action of "import".

The "Design Runs" window shows the following table:

Name	Elapsed	FMax (MHz)	Util (%)	Status	Progress	Part	Constraints	Strategy
config_1	00:00:31			Implementation Out-of-date	0%	xc4vx...	constrs_1	ISE Defaults
config_2 (active)	00:02:55	227.842	1	Implementation Out-of-date	100%	xc4vx...	constrs_1	ISE Default

The "Device" window shows a grid-based representation of the device configuration with modules like "recoModule1", "StaticModule1", and "recoModule2" placed on the grid.

# Partial Reconfiguration

PR\_BlinkDim\_with\_static - [~/data/Repository/CS/Partitions/PlanAhead/PR\_BlinkDim\_with\_static/PR\_BlinkDim\_with\_static.ppr] - PlanAhead 13.2

File Edit Flow Tools Window Layout View Help

Design Analysis

Implementation Out-of-date [more...](#)

Project Manager

Netlist Design

Resource Estimation  
Power Estimation  
Run DRC  
Report Timing  
Slack Histogram  
Set up ChipScope

Netlist Design - netlist\_1 - xc4vfx20ff572-11 (active)

Configurations

Configuration	Module Variant	Status
config_1 (4)		Implementation Out-of-date
Static Logic		Implement
recoModule2	blinkModule_Partition2	Implement
recoModule1	blinkModule_Partition1	Implement
staticModule1		Implement
config_2 (4)		Implementation Out-of-date
Static Logic		Import
recoModule2	dimModule_Partition2	Implement
recoModule1	dimModule_Partition1	Implement
staticModule1		Import

Project Summary x Device x

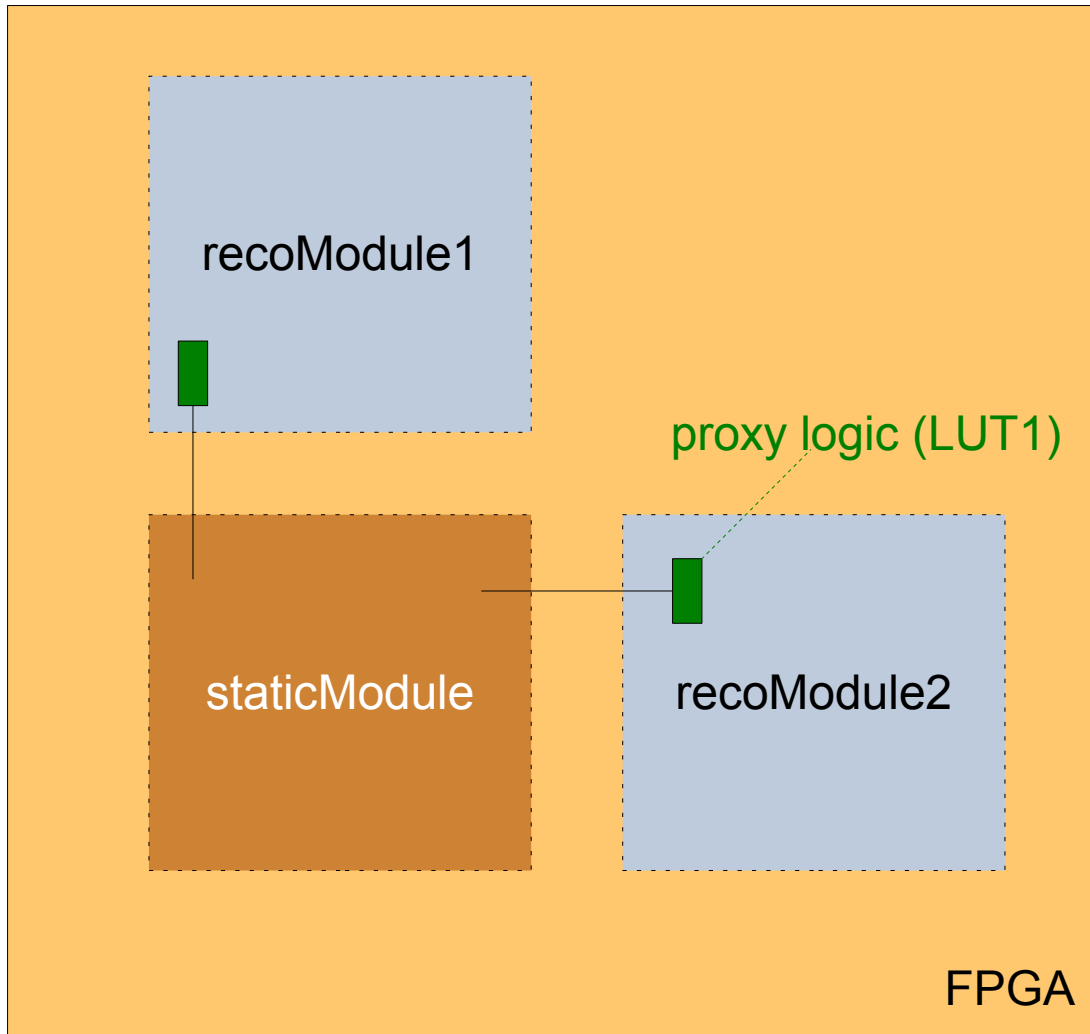
recoModule1  
recoModule2  
staticModule1

Part	Status	Progress	Part	Constraints	Strategy
1	Implementation Out-of-date	0%	xc4vfx...	constrs_1	ISE Defaults

Sources Netlist Configurations Timing Constraints..

1:1 Insert UCF Partial Reconfiguration Flow

# Partial Reconfiguration





# Partial Reconfiguration

Xilinx FPGA Editor - /data/Repository/CS/Fa-titions/PlanAhead/PR\_BlinkDim\_w\_th\_static/PR\_BlinkDim\_with\_static.runs/corfig\_1/config\_1\_routed.rcd

File Edit View Tools Window Help

Array1

\_list1

All Components

Name Filter

\*  Apply

	Name	Site	Type	#Pins	Hilita
1	bufgC	BUFGC	BUFG	2	no co
2	button[	KR	IOB	1	no co
3	button[	M6	IOB	1	no co
4	button[	L10	IOB	1	no co
5	button[	G11	IOB	1	no co
6	clk	AE14	IOB	1	no co
7	led[0]	F14	IOB	1	no co
8	led[1]	A10	IOB	1	no co
9	led[2]	F13	IOB	1	no co
10	led[3]	E10	IOB	1	no co
11	recoM	SLICE_SLICEL	5	no co	
12	recoM	SLICE_SLICEL	5	no co	
13	recoM	SLICE_SLICEL	7	no co	
14	recoM	SLICE_SLICEL	4	no co	

Word1

clicking on the apply button again.

For Help, press F1

xc4vx20-11f672 No Logic Changes Word Cards

# Partial Reconfiguration

Xilinx FPGA Editor - /data/Repository/CS/Fa-titions/PlanAhead/PR\_BlinkDm\_w th\_static/PR\_BlinkDim\_with\_static.runs/corfig\_2/config\_2\_routed.rcd

File Edit View Tools Window Help

Array1

\_list1

All Components

Name Filter

\*  Apply

	Name	Site	Type	#Pins	Hilita
1	bufgC	BUFGC	BUFG	2	no co
2	button[	KR	IOB	1	no co
3	button[	M6	IOB	1	no co
4	button[	L10	IOB	1	no co
5	button[	G11	IOB	1	no co
6	clk	AE14	IOB	1	no co
7	led[0]	F14	IOB	1	no co
8	led[1]	A10	IOB	1	no co
9	led[2]	F13	IOB	1	no co
10	led[3]	E10	IOB	1	no co
11	recoM	SLICE_	SLICEL	3	no co
12	recoM	SLICE_	SLICEL	3	no co
13	recoM	SLICE_	SLICEL	3	no co
14	recoM	SLICE_	SLICEL	3	no co

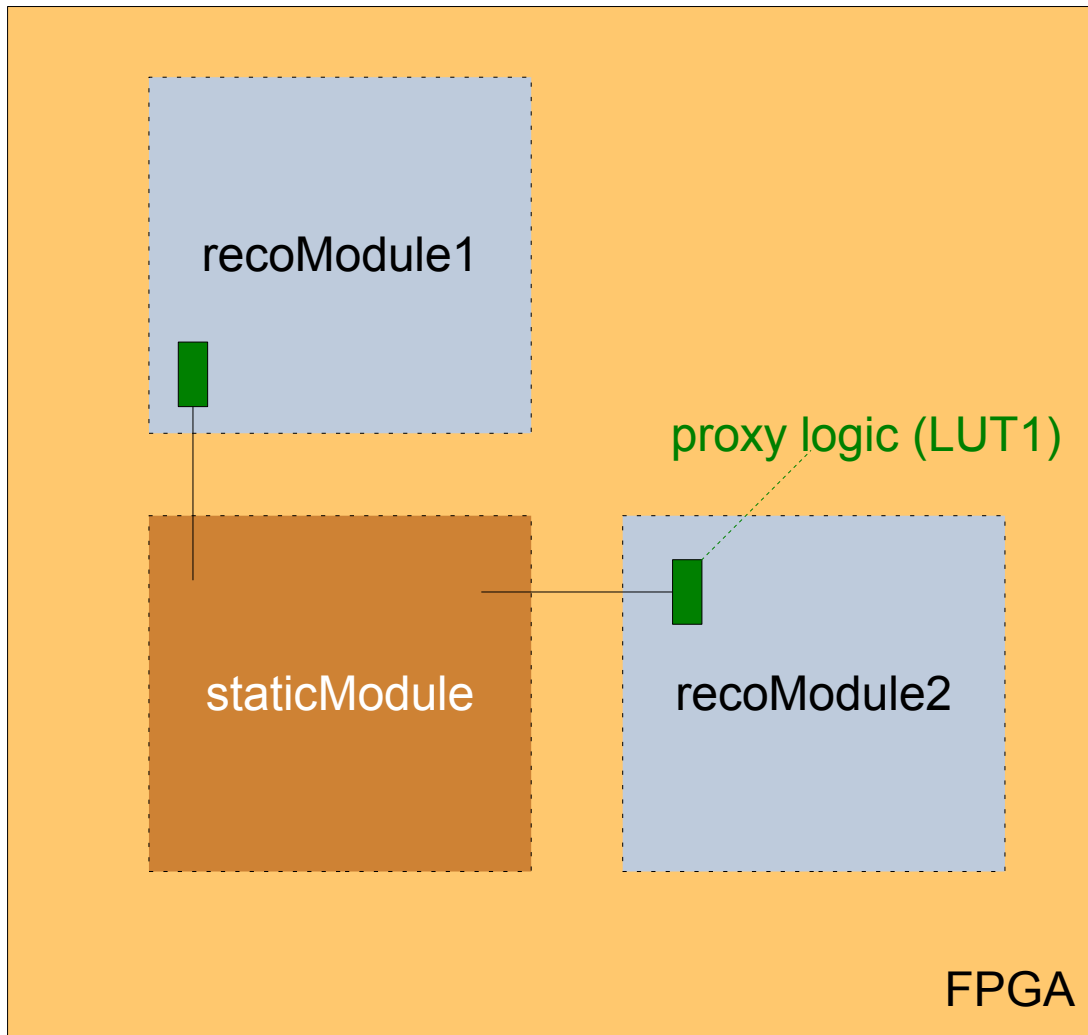
Word1

clicking on the apply button again.

For Help, press F1

xc4vx20-11f672 No Logic Changes Word Cards

# Conclusion



## Problems:

- Timing
- change of **static** Module causes rebuild of **all** Modules
- a Areas using m Modules  
=> m configurations  
=> m full implementation runs  
=> m full bitfiles  
=> a • m partial bitfiles
- no support of Spartan-6

## Our aims:

- clear Timing
- strict module separation
- movable bitfiles

# Questions?